■ TOPIC: THE DEMONSTRATION OF NOVEL SI VERTICAL NANO-WIRE/TUBE DEVICE

■ PRINCIPAL INVESTIGATOR (PI):

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- **Affiliation:** Department of Mechanical Engineering, National Taiwan University

■ PROPOSAL ABSTRCT:

The nano-wire (NW) device transistor architecture has been regarded as one of the most promising candidates for the sub-10/7 nm logic devices because the existing Fin field-effect transistors (Fin-FETs) still face the serious scaling limitation. However, the NW devices still have two big issues for the real production based on our understanding. The first one is the process complexity of the continuous dimension scaling to meet the transistor's density on the fixed area chip. The second one is the serious trade-off between the carrier's transport mobility (I_{on}-state current) and the short channel control (I_{off}-state current). The NW transistor with the smaller diameter (d) dimension leads to the better short channel control but suffers the degradation of the carrier transport mobility due to the serious surface roughness scattering (as shown in the Fig. 1). **In this proposal**, the **vertical gate-all-around (V-GAA) Si nano-tube (NT) device structure** (as shown in the Fig. 1) is proposed and will be demonstrated with the promising device performance and short channel control. The **V-GAA** structure can effectively increase the transistor's density on the fixed area chip. The **NT** device with the center hollow structure can lead to the better short channel control without the degradation of the carrier transport mobility by "screening-out" and "depleting" the out-of gate control carriers in the center of the NW device. Compared to the traditional lateral NW device with the smaller d (d≦10 nm), the proposed **V-GAA NT** device has the highly potential and an advantage to increase the transistor's density on the fixed chip area and have the better short channel control based on the theoretical calculation. Fig. 2 and Fig. 3 show our designed process flow and the initial device demonstration with the observation of transmission electron microscope image and electrical measurement. It shows that **our proposed NT device with the hollow structure indeed can "screen-out" and deplete the out-of gate control carriers to benefit the short channel control and I_{off}-state current reduction**. **With the support from this project, we reasonably expect that the proposed vertical gate-all-around (V-GAA) Si nano-tube (NT) device with the better device performance can further be demonstrated that it is indeed one of the highly potential candidates to replace the current Si FinFET device structure in the nearly coming future.**

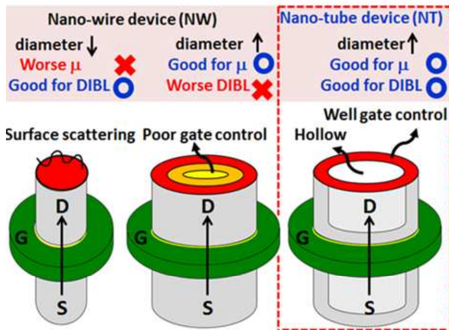
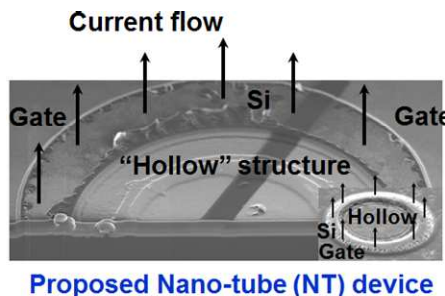


Fig. 1 The proposed vertical nano-tube device structure.



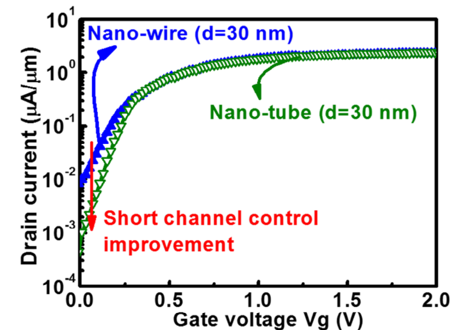


Fig. 3 The initial NT experimental data of TEM image and electrical measurement.

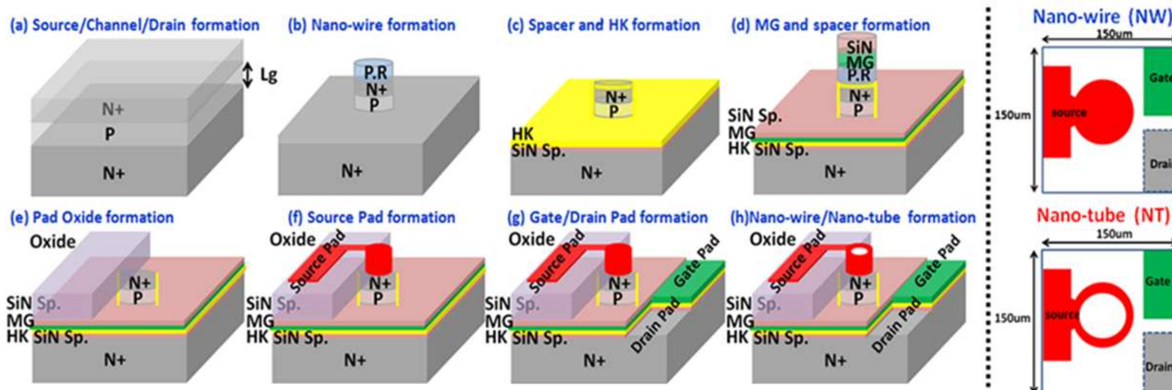


Fig. 2 The designed device process flow for the proposed vertical nano-wire/tube device structures.

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SUMMARY OF QUALIFICATIONS

- A device specialist/technical leader in TSMC and prestigious scholar/professor (tenure) in NTU with 11 years of working experience in CMOS logic transistor development.
- Proven ability to work on teams, communicate effectively and manage the large complex research/development projects with customers, specifically for the foundry business.

EDUCATION

- **PhD** in Electrical Engineering, National Taiwan University, Taiwan. **7/2007**
- **Double-BS** in Mechanical/Electrical Engineering, National Taiwan University, Taiwan. **7/2003**

RELEVANT EXPERIENCE

- **Associate Professor (with tenure)** in National Taiwan University, Taiwan. **10/2011-present**
  - Publish 100+ technical papers in top conference proceedings and international journals such as IEDM and VLSI, mainly in the field of advanced transistor developments along with 10+ patents.
  - Demonstrate the high device performances of Ge (VLSI 2014)/III-V MOSFETs, steeper slope transistors with negative capacitance effect and low power consumption (IEDM 2015/2016), vertical nano-wire/tube devices (JAP), and magnetic spin-electronics (VLSI 2014).
  - Manage international research programs and groups with ~50+ researchers.
- **Principal Engineer and Team Leader** in Module/Device Engineering/Process Integration, R&D, Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan. **7/2005-10/2011**
  - Device performance boost and analysis, SPICE modeling and targeting, TCAD simulation, Exploratory Device Path-finding and Design, Layout effect investigation, Yield improvement, and NTO shuttle lots arrangement in 40HP/32G/28HP/16 nm technology node devices.
  - Take the responsibility to manage the project and co-work/negotiate with the customer for the foundry business (28 HP+ project for the fujitsu's super computer).
  - Transfer R&D projects to Fab 12A/B in TSMC for the mass production and yield improvement.

ACTIVITIES

- The **Secretary-General** in Chinese Institute of Engineers, Taipei, Taiwan. **12/2011-12/2015**
- **Member**, IEEE. **12/2003-present**

SKILLS

- **Technical**: Solid-State Devices and Semiconductor Engineering, Rich international experience in managing large complex research and development projects with customers
- **Languages**: Mandarin (native), Taiwanese (native), English (fluent)

HONORS

- TSMC Research Special Bonus Award (with-in top 2%) in 2010 and the Best TSMC Patent Award in 2011.
- NTU Young Researcher Award in 2014 and the Outstanding Young Persons of Taiwan Merit Award in 2015.

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REFERENCES

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Dr. Ieong was program director when I worked on the development of 28 nm High-Performance and Mobile Logic Device Technologies. He recognized my outstanding contribution to the success of 28 nm device engineering and international management experience in large complex research/development projects with customers, for the foundry business specifically. Prior to joining TSMC, he was the senior manager at IBM T.J. Watson Research Center.

- Dr. Mong-Song Liang, IEEE Fellow, Vice Present in R&D

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Dr. Liang was senior program director when I worked on the development of 40/32 nm Logic Device Technologies. He recognized my outstanding contribution to the success of 40/32 nm device/integration/module engineering. Prior to joining TSMC, he was the senior manager at Advanced Micro Devices, Inc. (AMD).

- Dr. Chung-Hsun Lin, IEEE Senior Member, Director in R&D

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Dr. Lin has the close interaction and discussion with me on some common research topics in the international conference. He recognized my outstanding contribution to the development of advanced logic devices such as Ge FET, III-V FET, and Magnetic Spin-electronics in the academic society. Prior to joining GLOBALFOUNDRIES, he was the senior manager at IBM T.J. Watson Research Center.