■ TOPIC: THE INVESTIGATION FOR THE REDUCTION OF S/D METAL CONTACT RESISTANCE IN HIGH PERFORMANCE 2D MoS_2 DEVICE

■ PRINCIPAL INVESTIGATOR (PI):

- **Name:** Ming-Han Liao (E-mail/Phone: mhliaoa@ntu.edu.tw/886-918-936-625)
- **Affiliation:** Department of Mechanical Engineering, National Taiwan University

■ PROPOSAL ABSTRCT:

2D Material devices (**Molybdenum disulfide** (MoS_2)) has been regarded as one of high potential device structures/materials to replace the current Si FinFET devices, due to its capability to be continuously scaled down the device dimension. However, the main bottleneck for the development of 2D device is the high Source/Drain contact resistance, due to the high Schottky barrier height between the contact metal and TMD – MoS_2 channel. **In this proposal, we want to investigate and analysis the MoS_2 2D device performance with different contact metals and discuss the in-depth physics further to reduce the S/D contact resistance. With the close co-work with Prof. Lance Li in KAUST by using chemical vapor deposition (CVD) to deposit MoS_2 thin film as ultra-thin channel materials** (as shown in the Fig.1), we make the 2D field effect transistor (FET) successfully, which is notable similar to an UTB device. With the deposition of different work functions (ϕ_m) metals by using sputter technique, we have fabricated and demonstrated the high performance MoS_2 devices with different S/D contact metals. In our proposal, the **top-contact** structure in the 2D device is demonstrated (as shown in the Fig. 2) by the proposed process flow (as shown in the Fig. 3). **The DFT simulation on TMD device shows that the conversion of 2H semiconducting to 1T metallic states is existed at the contact junction**. Top-contact structure ensures the connection of electron to all the layers of 2DM. **In this proposal, we want to demonstrate that the pure top-contact structure not only greatly reduces the contact resistance through the metallized 2D material but also can easily be integrated in the current process of semiconductor manufacturing** (as shown in the Fig. 4). **We also plan to deposit different dielectric thin film on this kind of 2D materials to isolate our ultra-thin channel from an environment.** For example, **using hBN dielectric material to form a dielectric environment can restrict the electron flowing only in the 2D channel material. 2D material device indeed can greatly reduce the chip size and save the power consumption in the real electrical product. This kind of technique has been demonstrated to be a highly potential candidate to replace the current channel material Si in the nearly coming future.**

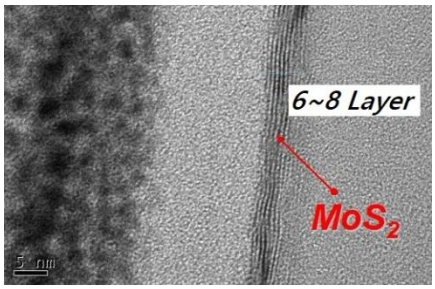

Fig. 1 The SEM image on our MoS_2 thin film, which is deposited by CVD.

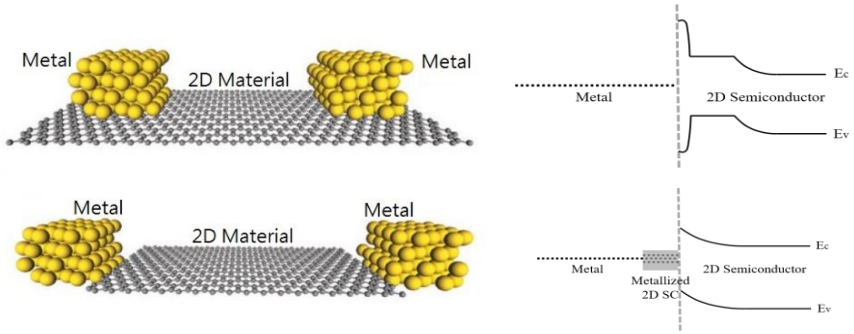

Fig. 2 Two different contact structures: Top-contact (up) and Edge-contact (down) in 2D devices.

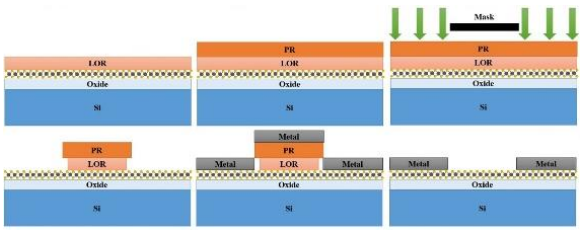

Fig. 3 The developed lift-off process for the top-contact 2D device.

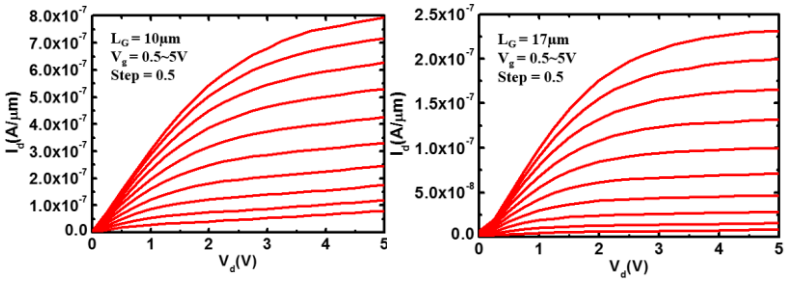

Fig. 4 2D MoS_2 device performance demonstration with Pd contact in the top-contact device structure.

Ming-Han (Milton) Liao

2723 South State St. STE 150 Ann Arbor, MI 48104 (U.S.) (Expect to have Permanent Residence on July, 2017)
14F, No.386, Pu-ding 1st Rd., East Dist., Hsin-chu City 300, Taiwan (R.O.C.)
(E-mail) mhliaoa@ntu.edu.tw ; **(Phone)** +886-918-936-625

SUMMARY OF QUALIFICATIONS

- A device specialist/technical leader in TSMC and prestigious scholar/professor (tenure) in NTU with 11 years of working experience in CMOS logic transistor development.
- Proven ability to work on teams, communicate effectively and manage the large complex research/development projects with customers, specifically for the foundry business.

EDUCATION

- **PhD** in Electrical Engineering, National Taiwan University, Taiwan. **7/2007**
- **Double-BS** in Mechanical/Electrical Engineering, National Taiwan University, Taiwan. **7/2003**

RELEVANT EXPERIENCE

- **Associate Professor (with tenure)** in National Taiwan University, Taiwan. **10/2011-present**
  - Publish 100+ technical papers in top conference proceedings and international journals such as IEDM and VLSI, mainly in the field of advanced transistor developments along with 10+ patents.
  - Demonstrate the high device performances of Ge (VLSI 2014)/III-V MOSFETs, steeper slope transistors with negative capacitance effect and low power consumption (IEDM 2015/2016), vertical nano-wire/tube devices (JAP), and magnetic spin-electronics (VLSI 2014).
  - Manage international research programs and groups with ~50+ researchers.
- **Principal Engineer and Team Leader** in Module/Device Engineering/Process Integration, R&D, Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan. **7/2005-10/2011**
  - Device performance boost and analysis, SPICE modeling and targeting, TCAD simulation, Exploratory Device Path-finding and Design, Layout effect investigation, Yield improvement, and NTO shuttle lots arrangement in 40HP/32G/28HP/16 nm technology node devices.
  - Take the responsibility to manage the project and co-work/negotiate with the customer for the foundry business (28 HP+ project for the fujitsu's super computer).
  - Transfer R&D projects to Fab 12A/B in TSMC for the mass production and yield improvement.

ACTIVITIES

- The **Secretary-General** in Chinese Institute of Engineers, Taipei, Taiwan. **12/2011-12/2015**
- **Member**, IEEE. **12/2003-present**

SKILLS

- **Technical**: Solid-State Devices and Semiconductor Engineering, Rich international experience in managing large complex research and development projects with customers
- **Languages**: Mandarin (native), Taiwanese (native), English (fluent)

HONORS

- TSMC Research Special Bonus Award (with-in top 2%) in 2010 and the Best TSMC Patent Award in 2011.
- NTU Young Researcher Award in 2014 and the Outstanding Young Persons of Taiwan Merit Award in 2015.

Ming-Han (Milton) Liao
2723 South State St. STE 150 Ann Arbor, MI 48104 (U.S.) (Expect to have Permanent Residence on July, 2017)
14F, No.386, Pu-ding 1st Rd., East Dist., Hsin-chu City 300, Taiwan (R.O.C.)
(E-mail) mhliaoa@ntu.edu.tw ; **(Phone)** +886-918-936-625

REFERENCES

- Dr. Meikei Ieong, IEEE Fellow, Chief Technology Officer (CTO)

Hong Kong Applied Science and Technology Research Institute (ASTRI)
3/F, Bio-informatics Centre, 2 Science Park West Avenue
Hong Kong Science Park, Shatin, Hong Kong
Direct +852-3406-2549
mkieong@astri.org

Dr. Ieong was program director when I worked on the development of 28 nm High-Performance and Mobile Logic Device Technologies. He recognized my outstanding contribution to the success of 28 nm device engineering and international management experience in large complex research/development projects with customers, for the foundry business specifically. Prior to joining TSMC, he was the senior manager at IBM T.J. Watson Research Center.

- Dr. Mong-Song Liang, IEEE Fellow, Vice Present in R&D

Samsung Electronics
Samsung Plaza Bldg 263 Seohyeon-Dong,Bundang-Gu, Seongnam City, Gyeonggi-Do,463-721 Korea
kindmsliang@yahoo.com.tw (***private*** E-mail address)

Dr. Liang was senior program director when I worked on the development of 40/32 nm Logic Device Technologies. He recognized my outstanding contribution to the success of 40/32 nm device/integration/module engineering. Prior to joining TSMC, he was the senior manager at Advanced Micro Devices, Inc. (AMD).

- Dr. Chung-Hsun Lin, IEEE Senior Member, Director in R&D

Advanced Technology Development at GLOBALFOUNDRIES
2070 Route 52, Fishkill, NY 12533, U.S.
chunghsunlin@gmail.com (***private*** E-mail address)

Dr. Lin has the close interaction and discussion with me on some common research topics in the international conference. He recognized my outstanding contribution to the development of advanced logic devices such as Ge FET, III-V FET, and Magnetic Spin-electronics in the academic society. Prior to joining GLOBALFOUNDRIES, he was the senior manager at IBM T.J. Watson Research Center.