InAlP-Capped (100) Ge nFETs with 1.06 nm EOT: Achieving Record High Peak Mobility and First Integration on 300 mm Si Substrate

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I. Introduction

Ge is a promising alternative channel material for sub-10 nm CMOS technology due to its high electron and hole mobilities. Ge pFETs with excellent subthreshold characteristics and high drive current I_{ON} have been demonstrated [1]. While various surface passivation techniques have been reported for Ge nFETs [2]-[19], realizing Ge nFETs with small subthreshold swing S and high I_{ON} is still challenging, especially for enhancement mode Ge nFETs. In addition, Ge nFETs should preferably be formed on Si substrates.

In this work, InAlP-capped Ge nFETs were realized on 300 mm Si substrates using the buffer layer technique for the first time. With a gate stack comprising 2.3 nm of InAlP and 2 nm of HfO_2, an EOT of 1.06 nm was achieved. In addition, InAlP-capped Ge nFETs on bulk Ge substrates were also formed using sub-400 ºC process modules. At a gate length L_G of 3 µm, we obtained a record high Ge (100) peak mobility of 1370 cm^2/V·s, the lowest reported hysteresis of 15 mV, and S of 103 mV/decade. By scaling L_G down to 500 nm, the highest reported I_{ON} of 127 µA/µm (at $V_{GS} - V_{TH} = 1$ V and $V_{DS} = 1$ V) and peak intrinsic transconductance $G_{m,int}$ of ~275 µS/µm (at $V_{DS} = 0.8$ V) were obtained for enhancement mode Ge (100) nFETs.

II. Key Highlights and Device Fabrication

Key highlights of this work are shown in Fig. 1 (a). First, an InAlP passivation layer with a thickness of 2.3 nm was inserted between Ge and the high-*k* gate dielectrics for mobility enhancement. Second, a process flow with low thermal budget of 400 ºC was introduced to reduce the possible inter-diffusion among Ge, InAlP, and the gate dielectrics, and therefore maintains good interface quality. Third, scaling-down of EOT was realized by reducing the HfO_2 thickness or by direct deposition of HfO_2 on InAlP. Lastly, integration of Ge nFETs on 300 mm Si substrates was demonstrated for the first time.

The process flow for fabricating Ge nFETs is shown in Fig. 1 (b). A 2.3-nm thick InAlP layer was grown on the (100)-oriented Ge substrate by MOCVD. After pre-gate clean, 0.5 nm Al_2O_3 and 2 nm or 3 nm HfO_2 were deposited by ALD at a temperature of 250 ºC, followed by the TaN deposition and patterning. After S/D phosphorus implant, forming gas annealing (H_2:N_2 = 1:9) was performed at 400 ºC for 30 minutes. This step also activated the implanted phosphorus, and is the highest temperature step in the entire process flow (excluding InAlP growth). NiGe contact formation was finally performed at a temperature of 350 ºC to complete the transistor fabrication. For Ge nFETs integrated on the Si substrate, HfO_2 was directly deposited on InAlP without insertion of the Al_2O_3 layer. The Ge channel layer was grown on the 300 mm Si substrate using the buffer layer technique.

To illustrate the concept of inserting an InAlP passivation layer, Fig. 2 shows the energy band diagram of the InAlP-capped Ge nFETs at the strong inversion regime. There is a conduction band offset ΔE_C of 0.84 eV between InAlP and Ge. This ΔE_C value is large enough to confine the electrons in the Ge channel and separate them from the interface traps which may exist at the high-*k*/InAlP interface. This leads to reduced interface trap scattering, and therefore, higher drive current can be achieved.

III. InAlP-Capped Ge nFETs on the Ge Substrate

A. Long-Channel Ge nFETs

Fig. 3 shows the high resolution cross-sectional TEM image of the Ge/InAlP/Al_2O_3/HfO_2/TaN stack with InAlP of ~2.3 nm, Al_2O_3 of ~0.5 nm, and HfO_2 of ~2 nm. Excellent crystalline quality of the InAlP layer was observed. The Ge/InAlP and InAlP/Al_2O_3 interfaces are sharp and flat. Fig. 4 shows the EDX profile along the line A-A' in Fig. 3 and confirms the existence of In, Al, and P elements. The 'bumps' of the In and P EDX profiles also give the indication of the InAlP thickness of ~2.3 nm and is consistent with the one obtained from the TEM image in Fig. 3. RMS roughness of the InAlP-capped Ge surface is ~0.39 nm with a scan area of 3 µm × 3 µm, as indicated in the AFM image of Fig. 5.

I_{DS}-V_{GS} curves of a Ge nFET with L_G of 3 µm in Fig. 6 exhibits excellent transfer characteristics with S of 103 mV/decade and I_{ON}/I_{OFF} ratio close to 4 orders. The hysteresis is as small as 15 mV between forward and backward voltage sweeps. Reducing the HfO_2 from 3 to 2 nm leads to 8% enhancement of the drive current at V_{GS}-V_{TH} of 1 V and V_{DS} of 1 V, as shown in the I_{DS}-V_{DS} characteristics of the Ge nFETs with different HfO_2 thicknesses in Fig. 7. The cumulative statistical plot in Fig. 8 indicates that reducing the HfO_2 thickness from 3 to 2 nm also reduces the median S from 114 to 108 mV/decade.

Fig. 9 shows the electron effective mobility μ_{eff} of Ge nFETs as a function of inversion carrier density N_{INV} measured by the split-*CV* method. The effect of S/D series resistance R_{SD} was taken out during the mobility extraction. For Ge nFETs with the InAlP capping, record high electron peak mobility of 1370 $cm^2/V \cdot s$ was achieved on the (100)-oriented Ge substrate.

B. Interface Study of the Ge/InAlP/Al_2O_3/HfO_2 Stack

To extract the D_{it} of the Ge/InAlP/Al_2O_3/HfO_2 stack, Ge capacitors were fabricated. A thicker (5.5 nm) HfO_2 was used to reduce gate leakage so that D_{it} can be accurately extracted. Fig. 10 (a) and (b) show the *C-V* curves measured at different frequencies ranging from 1 kHz to 1 MHz at 230 K and 77 K, respectively. Using the conductance method, D_{it} with values ranging from 6.2×10^{11} to 2.5×10^{12} $cm^{-2}\cdot eV^{-1}$ near the valence band edge and mid-gap was obtained, as shown in the plot of D_{it} as a function of energy in the Ge band-gap (Fig. 11). Surface potential fluctuations in the Ge/InAlP/Al_2O_3/HfO_2 layers were considered during the extraction.

C. Electrical Characteristics of Short-Channel Ge nFETs

Output characteristics of a Ge nFET with L_G of 500 nm are shown in Fig. 12. I_{ON} of 127 μA/μm was obtained at $V_{GS} - V_{TH}$ of 1 V and V_{DS} of 1 V. This is the highest drive current reported for enhancement mode Ge (100) nFETs so far. I_{ON} of our Ge nFETs is limited by the high and un-optimized R_{SD}, which was extracted to be ~ 8 kΩ·μm. This is due to the non-self-aligned NiGe formation with large gap between the edge of the gate and the S/D contact pads. After taking out the effect of R_{SD} and drain conductance G_D, peak intrinsic $G_{m,int}$ of 275 μS/μm was achieved at V_{DS} of 0.8 V, as shown in the peak $G_{m,int}$ *vs.* L_G plot in Fig. 13.

IV. InAlP-Capped Ge nFETs on 300 mm Si Substrate

A. Growth of Ge Channel Layer on 300 mm Si Substrate

The Ge layer was grown on the Si substrate using the buffer layer technique by MOCVD. The buffer layer thickness is ~1 μm, as shown in the cross-sectional TEM image of Fig. 14 (a). The RMS surface roughness of the substrate after the growth of InAlP is ~0.51 nm with a scan area of 3μm × 3μm (not shown here). High resolution TEM image in Fig. 14 (b) shows the excellent crystalline quality of the InAlP layer and the uniform and sharp Ge/InAlP interface.

B. Electrical Characteristics Ge nFETs on the Si Substrate

Fig. 15 shows the I_{DS}-V_{GS} curves of a Ge nFET integrated on the Si substrate with *S* of 131 mV/decade. Drive current of 45.6 μA/ μm was obtained at V_{GS}-V_{TH} of 1 V and V_{DS} of 1 V (Fig. 16). Peak $G_{m,ext}$ at V_{DS} of 1.05 V as a function of L_G in Fig. 17 demonstrates good scalability of the InAlP-capped Ge nFETs. The *C-V* characteristics of the p-Ge/InAlP/HfO_2/TaN MOS capacitor in Fig. 18 shows that EOT of 1.06 nm was achieved with direct deposition of HfO_2 grown on 2.3 nm InAlP.

For Ge nFETs with the same L_G of 5 μm, the drive current measured at the same gate overdrive of 1 V and V_{DS} of 1 V is 2.5 times higher than that reported in Ref. 17 despite a larger EOT, as illustrated in Fig. 19. The gate leakage current density J_G in Fig. 20 is less than 3×10^{-2} A/cm^2 in the gate voltage range of -1 to 1 V. At V_{FB} + 1 V, J_G is only slightly larger than the smallest value reported, as indicated in the plot of J_G as a function of EOT in Fig. 21.

V. Benchmarking

Fig. 22 benchmarks the peak electron μ_{eff} of (100)-oriented Ge nFETs with various passivation techniques. The InAlP-capped Ge nFETs using sub-400 °C process modules achieve the record high Ge (100) electron peak mobility of 1370 $cm^2/V \cdot s$. In addition to the high μ_{eff}, InAlP-capped Ge nFETs also exhibit *S* comparable to the best reported values, as indicated in Fig. 23 where *S* values are plotted as a function of the EOT of long channel planar Ge nFETs. The benchmark of I_{ON} at $V_{GS} - V_{TH}$ of 1 V and V_{DS} of 1 V in Fig. 24 shows that a record high I_{ON} of 127 μA/μm for enhancement mode Ge nFETs was realized though the L_G is not the shortest.

VI. Conclusion

InAlP-capped Ge nFETs with sub-400 ºC process modules were reported. Ge nFETs on Ge substrates with InAlP/Al_2O_3/HfO_2 as gate dielectrics demonstrate the highest reported Ge (100) peak μ_{eff} for inversion mode devices. In addition, the gate stack with HfO_2 directly deposited on the InAlP cap was implemented in Ge nFETs on 300 mm Si substrates for the first time. This leads to the realization of long-channel Ge nFETs with 1.06 nm EOT, high drive current, excellent *S*, and low gate leakage current. InAlP is a good passivation technique for Ge nFET gate stack formation, and could enable the use of Ge channel for both nFETs and pFETs in future high performance and low power logic applications.

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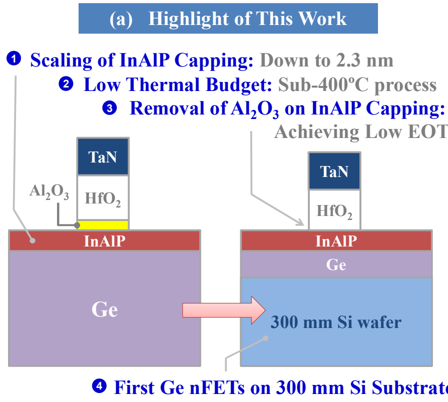

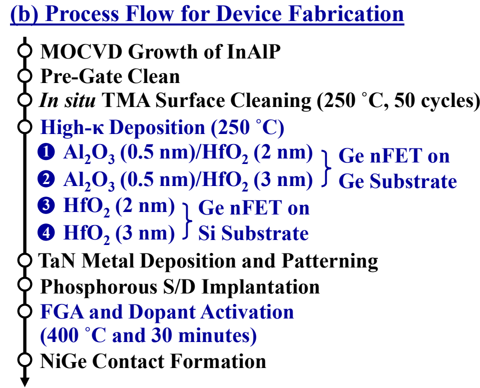

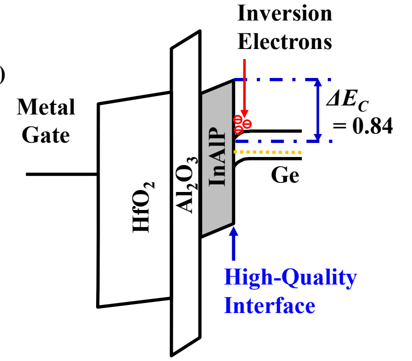

Fig. 1. (a) Key highlights of this work: An InAlP passivation layer with a thickness of 2.3 nm for mobility enhancement; Thermal budget is kept low to maintain a high-quality InAlP/Ge interface; EOT is scaled down by reducing HfO_2 thickness or by direct deposition of HfO_2 on InAlP; First integration of Ge nFETs on 300 mm Si substrate. (b) Key process steps for fabricating Ge nFETs. For Ge nFETs on Ge substrate, 0.5 nm of Al_2O_3 was used. For Ge nFETs integrated on Si substrate, no Al_2O_3 was used in the gate stack.

Fig. 2. Band diagram of an InAlP-capped Ge nFET at strong inversion regime. Electrons are confined in the Ge layer by the InAlP cap due to the large conduction band offset of 0.84 eV.

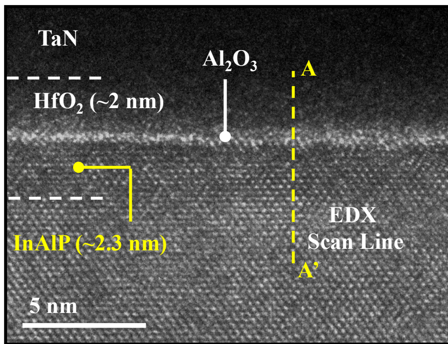

Fig. 3. High resolution cross-section TEM image of the Ge/InAlP/Al_2O_3/HfO_2/TaN stack. The InAlP and HfO_2 thicknesses are 2.3 and 2 nm, respectively. Excellent crystalline quality of InAlP, and sharp Ge/InAlP and InAlP/Al_2O_3 interfaces were observed.

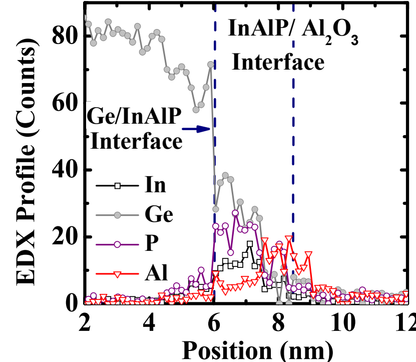

Fig. 4. EDX profile along the line A-A' in Fig. 3 confirms the InAlP grown on Ge. The InAlP thickness is ~2.3 nm and is consistent with the one obtained from the TEM image in Fig. 3.

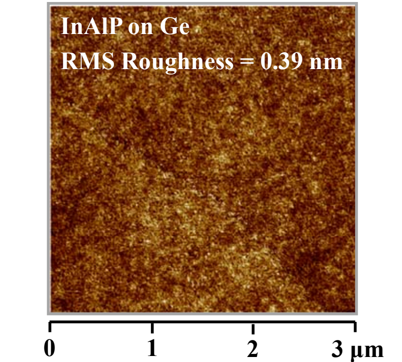

Fig. 5. RMS roughness of the InAlP-capped Ge surface is 0.39 nm with a scan area of 3µm×3µm.

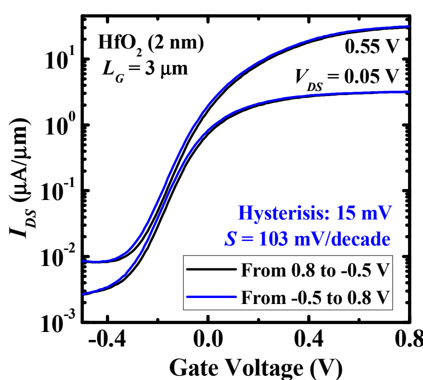

Fig. 6. Transfer characteristics showing S of 103 mV/decade, I_{ON}/I_{OFF} ratio close to 4 orders, and 15 mV hysteresis.

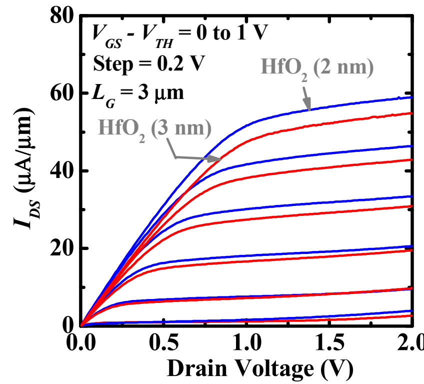

Fig. 7. Scaling HfO_2 from 3 nm to 2 nm enhances drive current by 8% at $V_{GS}-V_{TH}$ of 1 V and V_{DS} of 1 V.

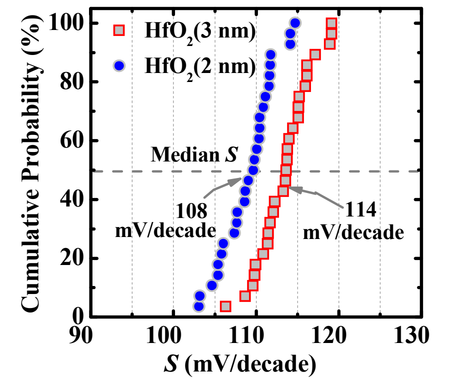

Fig. 8. Statistical plot shows tight distribution of S. Reducing the thickness of HfO_2 improves S.

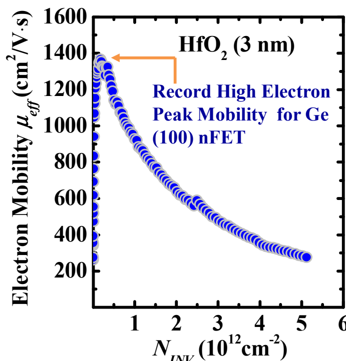

Fig. 9. Record high Ge (100) peak electron mobility of 1370 cm^2/V·s was achieved for the Ge nFETs with HfO_2 of 3 nm. S/D series resistance was corrected for the mobility extraction.

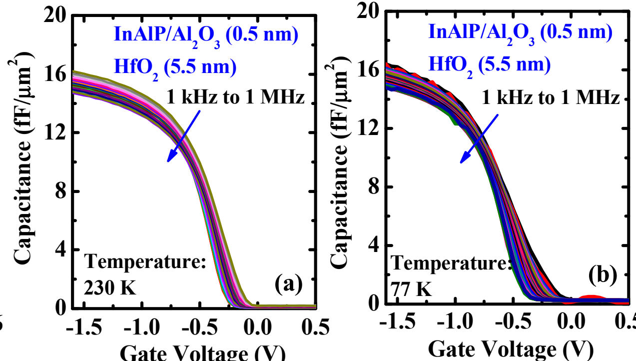

Fig. 10. C-V characteristics of the Ge MOS capacitors measured at (a) 230 K and (b) 77 K with different frequency values ranging from 1 kHz to 1 MHz.

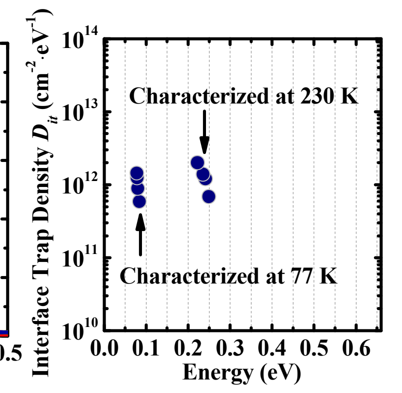

Fig. 11. D_{it} distribution near the valence band edge and mid-gap. D_{it} is in the range of 6.2×10^{11} to 2.5×10^{12} $cm^{-2}\cdot eV^{-1}$.

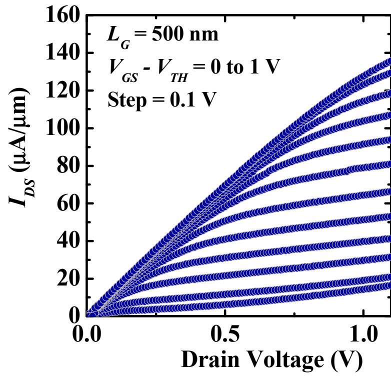

Fig. 12. I_{DS}-V_{DS} curves for a Ge nFET show I_{ON} of 127 μA/μm at $V_{GS} - V_{TH}$ of 1 V and V_{DS} of 1 V.

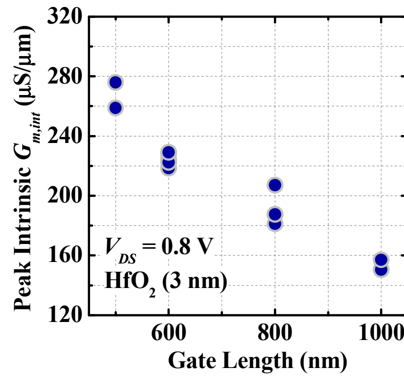

Fig. 13. Peak intrinsic $G_{m,int}$ of 275 μS/μm was achieved at V_{DS} of 0.8 V and L_G of 500 nm.

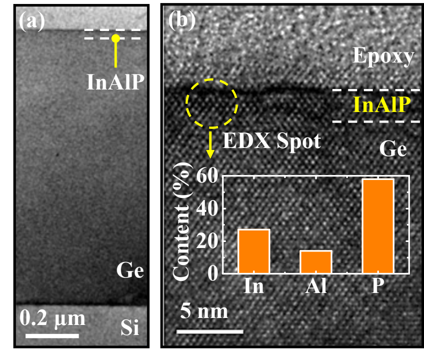

Fig. 14. (a) TEM image of an InAlP-capped Ge layer grown on 300 mm Si substrate. (b) High-resolution TEM showing the high-quality InAlP and the excellent InAlP/Ge interface.

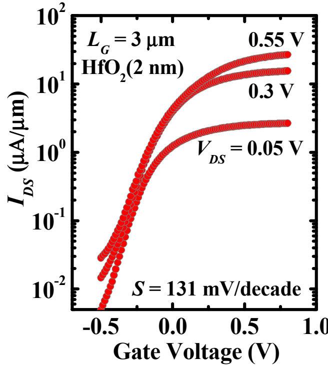

Fig. 15. The Ge nFETs on Si substrate show S of 131 mV/decade and I_{ON}/I_{OFF} ratio of more than 3 orders.

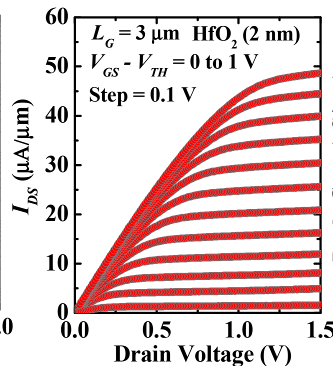

Fig. 16. Excellent pinch-off and saturation output characteristics were achieved for the same device in Fig. 15.

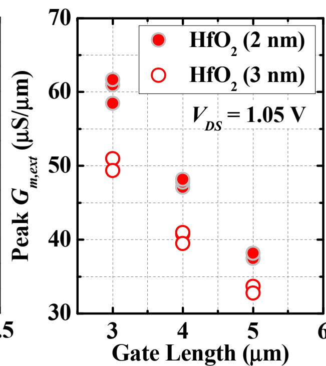

Fig. 17. Peak $G_{m,ext}$ of the Ge nFETs on Si substrate scale well with L_G. A thinner HfO_2 thickness improves peak $G_{m,ext}$.

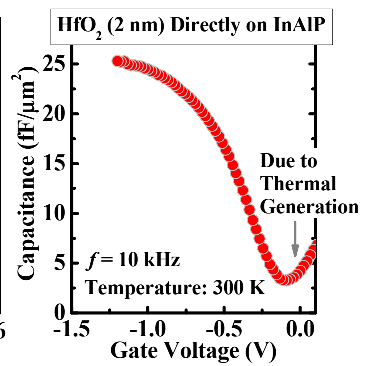

Fig. 18. C-V characteristics of the TaN/HfO_2/InAlP/p-Ge MOS capacitor. EOT of 1.06 nm was achieved.

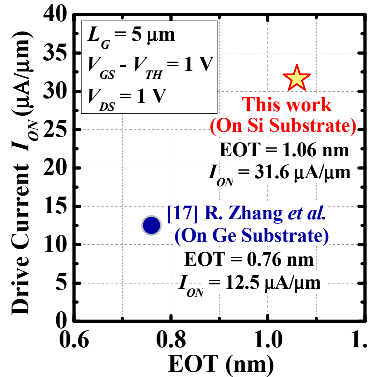

Fig. 19. Despite a larger EOT, the InAlP-capped Ge nFET on Si substrate shows 2.5 times higher I_{ON} as compared with that in Ref. 17 at the same L_G of 5 μm and the same $V_{GS} - V_{TH}$ of 1 V and V_{DS} of 1 V.

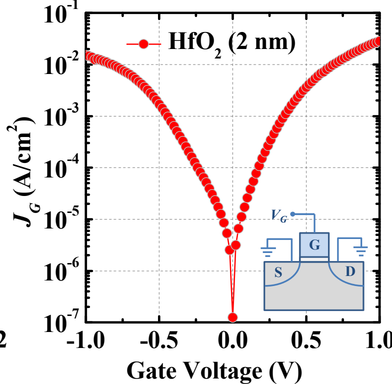

Fig. 20. J_G as a function of gate voltage for the Ge nFETs on the Si substrate with HfO_2 of 2 nm. The configuration for the measurement is also shown.

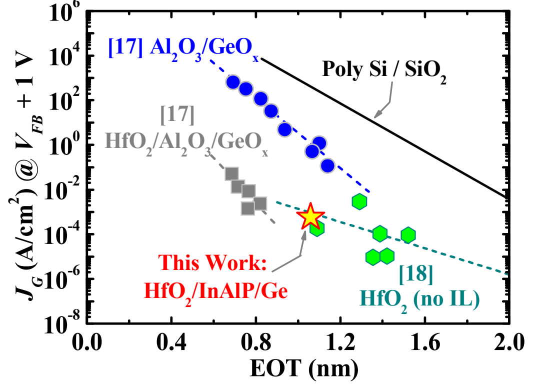

Fig. 21. J_G measured at V_{FB} + 1 V as a function of EOT. InAlP- capped Ge nFETs exhibit sufficiently suppressed gate current with EOT of 1.06 nm. This is attributable to the high-quality gate stack and maintaining of the physical thickness of gate dielectrics using HfO_2 with high permittivity.

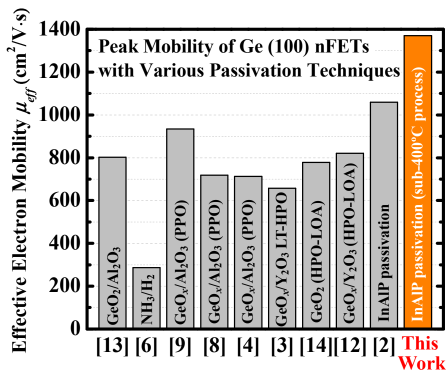

Fig. 22. Benchmark of peak μ_{eff} of Ge (100) nFETs using various passivation techniques in literature. Record high peak electron μ_{eff} of 1370 cm^2/V·s was achieved for Ge (100) nFETs in this work. Note that μ_{eff} of Ge (111) is not included.

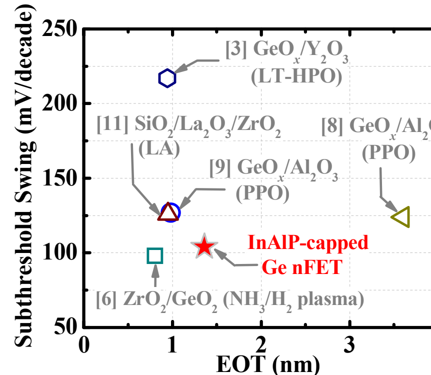

Fig. 23. S values as a function of EOT for long channel Ge nFETs with different surface passivation techniques. InAlP passivation leads to the realization of Ge nFETs with S comparable to the best reported values.

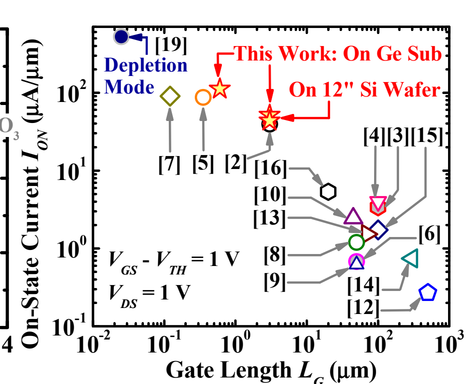

Fig. 24. Record high drive current of 127 μA/μm was achieved for enhancement mode Ge nFETs at $V_{GS} - V_{TH}$ of 1 V and V_{DS} of 1 V though the L_G is not the shortest. Note that Ref. 19 is a depletion-mode device.