Systematic Investigation of Self-Heating Effect on CMOS Logic Transistors From 20 to 5 nm Technology Nodes by Experimental Thermoelectric Measurements and Finite Element Modeling

M.-H. Liao, C.-P. Hsieh, and C.-C. Lee

***Abstract*— The characteristics of thermal conductivity (k) with different operated temperatures (T), material thicknesses (t), and impurity concentrations (N) are studied by thermoelectric measurements and developed simulation model for the study of self-heating effect. With the input of these module-level material properties in our developed finite-element model, the self-heating effect on the CMOS logic transistors from 20- to 5-nm technology nodes are investigated systematically and accurately. The maximum chip temperature in the 14/16-nm technology node Si FinFET device is ∼170 °C. On the other hand, the higher operated temperature is also observed in high mobility material devices such as Ge and III-V (InAs) FinFETs due to their poor material properties of k-value. It indicates that these high mobility materials are hard to be used in the next generation scaled technology node devices, unless these devices can be operated at the ultralow voltage bias (<0.5 V for InAs and <0.8 V for Ge) from the self-heating effect point of view.**

***Index Terms*— CMOS Logic transistors, self-heating effect, Si FinFETs.**

I. Introduction

SELF-HEATING effect in the CMOS logic transistors is becoming increasingly important, when the dimension of the device is continuously scaled down. The higher operated temperature in the chip results in many trouble issues including device performance variation [1], the increase of the OFF-state current (I_{OFF}) [2], and the worse device reliability [1]. Recently, many different research groups have studied this effect by theoretical calculation [3], experimental setup for the self-heating effect observation [4]–[7], and the brief discussion of self-heating effect on the Si device [8]. On the other hand, high mobility material devices, such as Ge [9]–[11] and III-V [12], [13], MOSFETs are regarded as the highly potential candidates recently to replace the current Si-based device, due to their material characteristics having the higher carrier mobility. Therefore, the systematic investigation for the self-heating effect on Si (with different device structures/dimensions) and this effect on high mobility material devices are highly needed. In this brief, we develop the accurate simulation model with the calibration for the input of the extracted thermal conductivity (k) value experimentally to investigate the self-effecting effect on Si FinFETs with different device gate length (L_g), Fin height (H), Fin pitch (λ), and Fin width (W). The experimental infrared observation demonstrates that our simulation results are reasonable and consistent with the experimental data. The self-heating effect on high mobility devices, such as Ge and III-V (InAs) FinFETs, are also studied in this brief.

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II. Experiment

The k value, which is one of the most important key parameters for the self-heating effect study, is strongly dependent on different operated temperatures (T), material thicknesses (t), and impurity concentrations (N). In order to calibrate our developed finite-element simulation model for the self-heating effect to improve the accuracy, the k value is extracted experimentally by the designed thermoelectric measurements first [4] as shown in Fig. 1. The tested bridge structure is fabricated by the standard CMOS process.

A well calibrated 3-D device simulation deck is used for this brief where the source/drain and channel doping profiles of realized devices were extracted from Monte Carlo implant (atomistic) simulations. The simulated device structure for Si, Ge, and III-V (InAs) FinFETs can be referred to [14]–[16], respectively. Layout dimensions for 20- to 5-nm technology node CMOS logic transistors were taken from the predictive technology node roadmap. The simulation approach used in this brief is to extract the quasi-static temperature, which should be the cumulative rise in the peak temperature

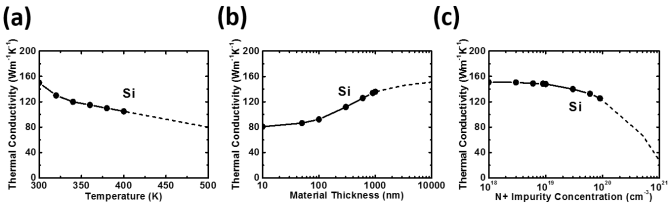

Fig. 1. The experimental extracted thermal conductivity dependency of (a) different operated temperature, (b) material thickness, and (c) impurity concentration in Si.

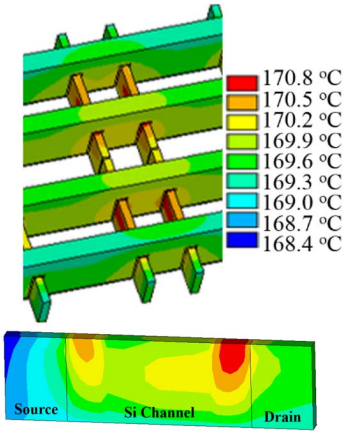

Fig. 2. Thermal characteristics with temperature distribution in the real Si devices. It can be found that the simulated results are consistent and agree well with the experimental infrared measurement.

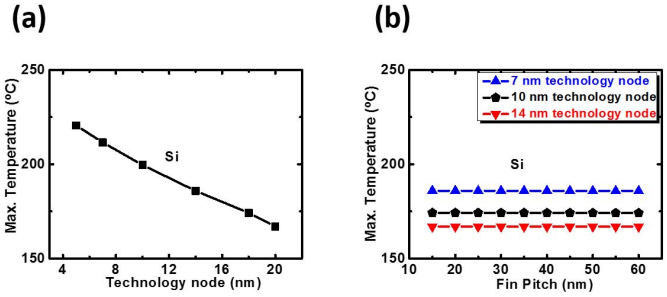

Fig. 3. Simulated maximum device temperature (T_{max}) dependence with (a) different technology nodes and (b) fin pitches in Si FinFET devices.

after 1000 s of pulses. Thermal properties of various regions are calibrated as per their exact dimensions and region-specific material used in a typical CMOS process flow.

III. Results and Discussion

Fig. 2 shows the thermal characteristics with temperature distribution in the real Si devices. It can be found that the simulated results are consistent and agree well with the experimental infrared measurement. The maximum chip temperature approaches to ~170 °C.

In Fig. 3, we investigate the self-heating effect and show the simulated maximum chip temperature in devices with different technology nodes from 20 to 5 nm and with different Fin pitches. When the device dimension is scaled down continuously, the chip temperature will be increased a lot (>200 °C in the 7-nm technology node device). The high operated

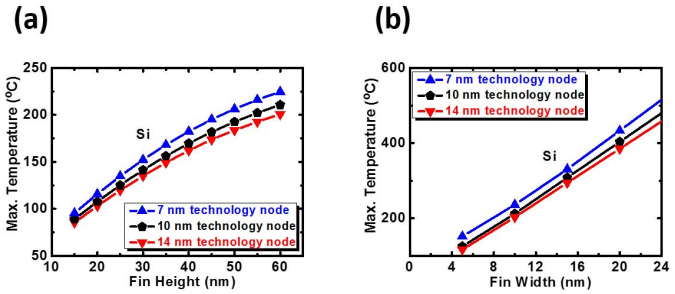

Fig. 4. Simulated maximum device temperature (T_{max}) dependence with (a) different Fin heights and (b) fin widths in Si FinFET devices.

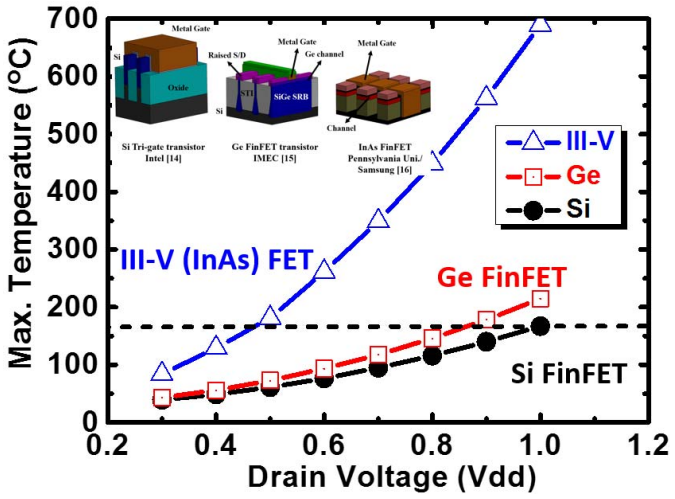

Fig. 5. Dependence of the maximum device temperature (T_{max}) with different voltage bias in Si, Ge, and III-V (InAs) FinFET devices. The simulated device structure/dimensions for Si, Ge, and III-V (InAs) FinFETs can be referred to [14]–[16], respectively.

temperature in the chip will lead to the device performance variation [1], the increase of the I_{OFF} [2], and the worse device reliability [1]. This phenomenon is called as self-heating effect and should be avoided in the real product in the industry.

Although the increase of the H and W in the Si FinFET device can increase the heat dissipation surface to further reduce the thermal resistance (R_{th}) possibly, the maximum operated temperature in the chip is still found to be increased as shown in Fig. 4, due to the simultaneous increase of the ON-state current (I_{ON}) per Fin, resulting in the increased power.

Besides the reduction of the Fin numbers [8], the most effective way to decrease this self-hating effect could be to reduce the operated voltage in the device. Fig. 5 simulates the maximum chip temperature with different voltage biases in Si, Ge, and III-V (InAs) FinFETs. The simulated device structure and dimension for Si, Ge, and III-V (InAs) FinFETs can be referred to [14]–[16] and also shown in the inset of Fig. 5, respectively. The technology node in these devices is 14, 45, and 40 nm, respectively.

Based on the simulation data, the operated chip temperature in the Ge and III-V (InAs) FinFET devices is found to be higher than it in the Si FinFET device due to the poor k value and thermal characteristics in these high mobility materials.

As we known, the k value of Si, Ge, and III-V (InAs) is $\sim$120 $\mathrm{Wm^{-1}K^{-1}}$, $\sim$80 $\mathrm{Wm^{-1}K^{-1}}$, and $\sim$10 $\mathrm{Wm^{-1}K^{-1}}$, respectively. This simulated result indicates that these high mobility materials are hard to be used in the next generation scaled technology node devices, unless these devices can be operated at the ultralow voltage bias (<0.5 V for InAs and <0.8 V for Ge) from the self-heating effect point of view.

IV. Conclusion

The accurate finite-element model, with the calibration of the experimentally extracted k parameters with different operated temperatures (T), material thicknesses (t), and impurity concentrations (N) in the module-level work, has been developed to investigate the self-heating effect on the CMOS logic transistors from 20- to 5-nm technology nodes. The simulated result of thermal characteristics in the Si FinFET device agrees well with the experimental observation by the infrared measurement. The maximum chip temperature in the 14/16-nm technology node Si FinFET device is up to $\sim$170 °C. The dependence of different device gate lengths (L_g), Fin height (H), Fin pitch (λ), and Fin width (W) in Si FinFET devices for the self-heating effect are also investigated in this brief. On the other hand, we also find that the operated chip temperature in the Ge and III-V (InAs) FinFET devices is higher than it in the Si FinFET device due to the poor k value and thermal characteristics in these high mobility materials. It indicates that these high mobility materials are hard to be used in the next generation scaled technology node devices, unless these devices can be operated at the ultralow voltage bias (<0.5 V for InAs and <0.8 V for Ge) from the self-heating effect point of view.

References

[1] S. W. Pae *et al.*, "Considering physical mechanisms and geometry dependencies in 14nm FinFET circuit aging and product validations," in *IEDM Tech. Dig.*, 2015, pp. 557–560.

[2] S. O. Koswatta *et al.*, "Off-state self-heating, micro-hot-spots, and stress-induced device considerations in scaled technologies," in *IEDM Tech. Dig.*, 2015, pp. 539–542.

[3] R. Rhyner and M. Luisier, "Self-heating effects in ultra-scaled Si nanowire transistors," in *IEDM Tech. Dig.*, 2013, pp. 790–793.

[4] M. Haras *et al.*, "Fabrication of integrated micrometer platform for thermoelectric measurements," in *IEDM Tech. Dig.*, 2014, pp. 212–215.

[5] S. Makovejev, S. H. Olsen, V. Kilchytska, and J.-P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–1851, Jun. 2013.

[6] S. H. Shin *et al.*, "Direct observation of self-heating in III–V gate-all-around nanowire MOSFETs," in *IEDM Tech. Dig.*, 2014, pp. 510–513.

[7] S. H. Shin *et al.*, "Direct observation of self-heating in III–V gate-all-around nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3516–3523, Nov. 2015.

[8] D. Jang *et al.*, "Self-heating on bulk FinFET from 14nm down to 7nm node," in *IEDM Tech. Dig.*, 2015, pp. 289–292.

[9] M.-H. Liao and S.-C. Huang, "The demonstration of promising Ge n-type multi-gate-field-effect transistors with the magnetic FePt metal gate scheme," *Appl. Phys. Lett.*, vol. 107, no. 4, pp. 092103–092107, Mar. 2015.

[10] M.-H. Liao and P.-G. Chen, "The dependency of different stress-level SiN capping films and the optimization of D-SMT process for the device performance booster in Ge n-FinFETs," *Appl. Phys. Lett.*, vol. 107, no. 5, pp. 072111–072115, Jun. 2015.

[11] M.-H. Liao and S.-C. Huang, "The demonstration of colossal magneto-capacitance effect with the promising gate stack characteristics on Ge (100) by the magnetic gate stack design," *Appl. Phys. Lett.*, vol. 104, no. 1, pp. 262406–262409, Jul. 2014.

[12] M.-H. Liao and L. C. Chang, "Experimental demonstration for the implant-free $\mathrm{In_{0.53}Ga_{0.47}As}$ quantum-well metal-insulator-semiconductor field-effect transistors with ultra-low source/drain resistance," *Appl. Phys. Lett.*, vol. 103, no. 4, pp. 072102–072106, Apr. 2013.

[13] R. Oxland *et al.*, "InAs FinFETs with $\mathrm{H}_{fin} = 20$ nm fabricated using a top-down etch process," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 261–264, Mar. 2016.

[14] S. Natarajan *et al.*, "A 14nm logic technology featuring 2^{nd}-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 $\mu\mathrm{m}^2$ SRAM cell size," in *IEDM Tech. Dig.*, 2014, pp. 71–74.

[15] L. Witters *et al.*, "Strained germanium quantum well p-FinFETs fabricated on 45nm Fin pitch using replacement channel, replacement metal gate and germanide-free local interconnect," in *VLSI Tech. Dig.*, 2015, pp. 56–57.

[16] A. V. Thathachary *et al.*, "Indium arsenide (InAs) single and dual quantum-well heterostructure FinFETs," in *VLSI Tech. Dig.*, 2015, pp. 208–209.