Spin MOSFETs as a Basis for Spintronics

SATOSHI SUGAHARA and MASAAKI TANAKA
The University of Tokyo

This article reviews a recently proposed new class of spin transistors referred to as spin metal-oxide-semiconductor field-effect transistors (spin MOSFETs), and their integrated circuit applications. The fundamental device structures, operating principle, and theoretically predicted device performance are presented. Spin MOSFETs potentially exhibit significant magnetotransport effects, such as large magneto-current, and also satisfy important requirements for integrated circuit applications such as high transconductance, low power-delay product, and low off-current. Since spin MOSFETs can perform signal processing and logic operations and can store digital data using both charge transport and spin degrees of freedom, they are expected to be building blocks for memory cells and logic gates in spin-electronic integrated circuits. Novel spin-electronic integrated circuit architectures for nonvolatile memory and reconfigurable logic employing spin MOSFETs are also presented.

Categories and Subject Descriptors: B.7.1 [**Integrated Circuits**]: Types and Design Styles—*Advanced technologies*

General Terms: Design, Performance, Reliability

Additional Key Words and Phrases: Spintronics, MOSFETs, spin transistors, spin MOSFETs

1. INTRODUCTION

Recently emerging spin-electronics (or spintronics) research [Prinz 1998; Wolf et al. 1991; Zutic et al. 2004], in which we try to utilize both charge transport and spin degrees of freedom for memory, logic, and signal-processing functions, is expected to have a great impact on semiconductor-integrated electronics. One of the most attractive directions being taken in this research field is manipulation of spin degrees of freedom in *active* semiconductor devices (i.e., transistor) and integrated circuits, while most of the studies on spin-electronics so far have been

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Authors' addresses: S. Sugahara, Department of Frontier Informatics, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan; email: sugahara@cryst.t.u-tokyo.ac.jp; M. Tanaka, Department of Electronic Engineering, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan; email: masaaki@ee.t.u-tokyo.ac.jp.

concentrated on new materials and related *passive* devices such as magnetic tunnel junctions and spin valves [Dieny 1994; Bass and Pratt 1999; Moodera and Mathon 1999; Dietl and Ohno 2003; Ohno 2004].

Spin transistors, which utilize two ferromagnetic layers as a spin injector and a spin detector, are considered to be candidates for such active devices. Ideally, spin transistors exhibit ordinary transistor actions with variable output characteristics that can be controlled by the relative magnetization configuration of the two ferromagnetic layers. In most spin transistors, the output current or transconductance (the output-current drive capability of the input voltage) of spin transistors can be switched by the relative magnetization configuration. This feature is often referred to as a magnetization-configuration-dependent output characteristic. In order to quantitatively express magnetization-configuration-dependent output characteristics, the magneto-current ratio (γ_{MC}) defined by $(I^{\mathrm{P}} - I^{\mathrm{AP}})/I^{\mathrm{AP}}$ where I^{P} and I^{AP} are the output currents in parallel and antiparallel magnetization configurations, respectively, is commonly used as the index of performance of spin transistors. Furthermore, the magnetization configuration of spin transistors can also be used as nonvolatile binary data. Owing to these useful features, spin transistors are potentially applicable to integrated circuits for ultrahigh-density nonvolatile memory whose memory cell is made up of a single spin transistor, and to nonvolatile reconfigurable logic based on multifunctional spin transistor gates. Although magnetization-configuration-dependent output characteristics are needed to realize such spin-electronic integrated circuits, device performance as a *transistor* is still important for spin transistors. Thus, the following requirements must be satisfied for spin transistors when they are used in integrated circuits as active devices:

(i) large magneto-current ratio (γ_{MC}) for nonvolatile memory and logic functions;
(ii) high transconductance (g_{m}) for high-speed operation;
(iii) high amplification capability (voltage, current, and/or power gains) to restore propagating signals between transistors and to realize large fan out;
(iv) small power-delay product and small off-current for low power dissipation;
(v) excellent scalability and simple device structure for a high degree of integration and high process yield.

After the proposal of the spin transistor concept by Datta and Das [1990] and Johnson [1993], various semiconductor-based spin transistors [Monsma et al. 1995; Jansen et al. 2004; Mizushima et al. 1997; van Dijken et al. 2002, 2003; Egues et al. 2003; Schliemann et al. 2003; Bandyopadhyay and Cahay 2006; Grundler 2001; Dennis et al. 2003; Fabian et al. 2004; Fabian and Zutic 2004; Flatte et al. 2003; Sugahara and Tanaka 2004; Sugahara 2005; Sugahara and Tanaka 2005; Ciuti et al. 2002; McGuire et al. 2004] which are analogous to ordinary nonmagnetic transistors [Sze 1981, 1990] such as a hot electron transistor (HET), modulation-doped field-effect transistor (MODEFT), bipolar junction transistor (BJT), and metal-oxide-semiconductor FET (MOSFET), have been

proposed so far. Nonvolatile data storage and magnetization-configuration-dependent output characteristics are the common features of these spin transistors. In many cases, however, their "transistor" performance that arises from their original constructions is sacrificed to realize these magnetization-related or spin-dependent transport features. Thus, it is important to explore spin transistors that simultaneously satisfy all the requirements noted above (items (i)–(v)).

The spin-valve transistor (SVT) [Monsma et al. 1995; Jansen et al. 2004] and magnetic tunnel transistor (MTT) [Mizushima et al. 1997; van Dijken et al. 2002, 2003] are HET-type spin transistor where a spin valve or a magnetic tunnel junction is employed in their device structures. These devices exhibit very large magneto-current ratios even at room temperature. However, the transfer ratio α ($=I_C/I_E$, where I_E is the emitter current and I_C is the collector current) of SVT and MTT reported so far is extremely low ($<10^{-3}$). It would be difficult for these devices to achieve high transconductance and also current gain due to the tradeoff between the magneto-current ratio and transfer ratio, which severely restricts their integrated circuit applications.

The spin field-effect transistor (spin FET) proposed by Datta and Das [1990], and its modified versions by Egues et al. [2003] and Schliemann et al. [2003], which consists of a modulation-doped channel structure and ferromagnetic source/drain contacts, might be expected to have an equally high transconductance and high cut-off frequency as conventional MODFETs due to the similarity in device structure. Using a gate-bias-induced Rashba spin-orbit interaction, the on/off-state of the spin FET can be controlled by the spin precession angle (0 or π) of the spin-polarized carrier transported from the source-side edge of the channel to the drain-side edge of the channel. This leads to unique transistor actions: When the relative magnetization configuration of the ferromagnetic source/drain is fixed, the on/off-state is cyclically turned by the gate bias. This feature is very useful to realize rather complex logic functions such as EXOR. On the other hand, when the gate bias is fixed, the output current can be modulated by the relative magnetization configuration of the ferromagnetic source/drain. This is attractive to non-volatile memory application. However, the transistor operation by the Rashba spin-orbit interaction deteriorates the transistor performance (transconductance and cut-off frequency) of MODFETs [Bandyopadhyay and Cahay 2004], and scaling merits cannot be expected in this device because significantly long channel length ($\sim 1\mu$m) is required for large spin precession ($>\pi$) [Bandyopadhyay and Cahay].

The magnetic bipolar transistor (MBT) proposed by Fabian et al. [2004], Fabian and Zutic [2004], and Flatte et al. [2003] is a BJT-type spin transistor whose base region is made up of a ferromagnetic seminconductor. The spin-dependent built-in potential at the emitter-base pn junction leads to magnetization-configuration-dependent output characteristics when a ferromagnetic spin injector is used for the emitter contact [Fabian et al. 2004; Fabian and Zutic 2004]. Large magneto-current, high transconductance, and high current gain are theoretically predicted. Although MBT is considered to be suitable for high-speed integrated circuits as well as conventional BJTs, its large power dissipation or large power-delay product would restrict integration

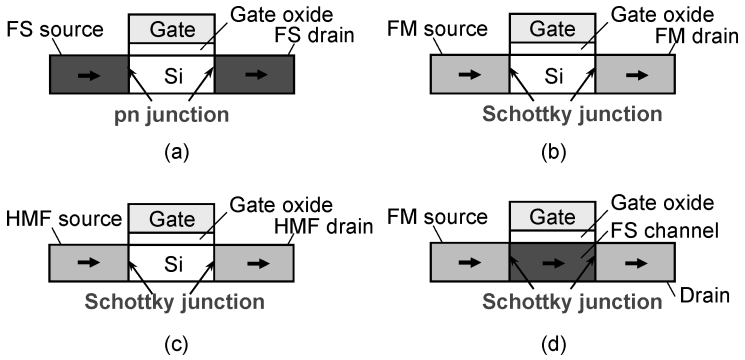

Fig. 1. Different types of spin MOSFETs with (a) a ferromagnetic semiconductor (FS), (b) a ferromagnetic metal (FM), and (c) a half-metallic ferromagnet (HMF) for the source/drain. A spin MOSFET with the FS channel and the FM (or HMF) source/drain is also shown in (d).

density. Thus, it is considered unsuitable for ultrahigh-density memory and mobile electronics applications.

In this article, recently proposed new MOSFET-type spin transistors [Sugahara and Tanaka 2004; Sugahara 2005; Sugahara and Tanaka 2005], hereafter referred to as spin MOSFETs, and their integrated circuit applications are reviewed. The article is organized as follows: In Section 2, we provide fundamental structures of various spin MOSFETs that are classified by the structure of source/drain and channel. Possible materials to realize them are also described. In Section 3, we present the operating principle and the theoretically predicted device performance of a spin MOSFET, concentrating on the spin MOSFET using half-metallic ferromagnet contacts for the source/drain. In Section 4, we provide novel spin-electronic integrated circuit architectures for nonvolatile memory and reconfigurable logic using spin MOSFETs. In Section 5, we summarize our conclusions.

2. CLASSIFICATION OF SPIN MOSFETs

The basic structure of spin MOSFETs consists of an MOS capacitor and a ferromagnetic source and drain [Sugahara 2005]. The source and drain of the spin MOSFETs should have ohmic-like contacts to the channel when the transistor is in the on-state, and they should also be contacts for blocking leakage current when the transistor is in the off-state. These features are essential for large on-current (high transconductance) and small off-current (low power). Schottky or pn junctions are commonly used source/drain contacts in ordinary MOSFETs. In order to realize magnetization-configuration-dependent output characteristics, a ferromagnetic character must be introduced into the source/drain (and channel) of spin MOSFETs. Figure 1 schematically shows different types of spin MOSFETs, which can be classified by the structure of the source/drain and channel.

The simplest way to obtain a spin MOSFET structure is to replace the source/drain material of an ordinary MOSFET with a ferromagnetic semiconductor (FS) that forms a ferromagnetic pn junction with the Si channel,

as shown in Figure 1(a). Possible candidates for source/drain materials are group-IV-based FSs, that is, Si, Ge, and SiGe doped with magnetic irons [Araki et al. 2002, 2003; Stroppa et al. 2003; Park et al. 2002; D'Orazio et al. 2003; Cho et al. 2002; Tsui et al. 2003; Shuto et al. 2006] (as described later in detail). Since only a small spin-valve-like magnetoresistive effect is expected in the carrier transport from the source to drain if the spin polarization of an FS is moderate, an FS with a large spin polarization must be used to obtain large magneto-current.

Figure 1(b) schematically shows a spin MOSFET using ferromagnetic Schottky contacts for the source/drain. The structure of the spin MOSFET is similar to that of Schottky barrier MOSFETs [Lepselter and Sze 1968; Hattori et al. 1992; Hattori and Shirafuji 1994] except for the Schottky contact material of a ferromagnetic metal (FM). This type of spin MOSFET can be operated as an accumulation- and inversion-type channel device. Possible materials for the source/drain are FMs with large spin polarization. CoFe and CoFeB are commonly used in magnetic tunnel junctions as the ferromagnetic electrodes, which exhibit large tunneling magnetoresistance, indicating large spin polarization [Han et al. 2002; Wang et al. 2004]. Fe_3Si is also an attractive candidate [Herfort et al. 2003; Nakane et al. 2006]. Recently, relatively high spin injection from Fe_3Si into a semiconductor was reported using an Fe_3Si/GaAs Schottky junction [Ramsteiner et al. 2004]. Note that one of the important challenges is to realize low Schottky barrier height (typically less than 0.2 eV) for large magneto-current and high transconductance of the spin MOSFET. When the tunneling emission through the Schottky barrier is used for injection of carriers from the source to the channel, relatively large magneto-curret ratios can be expected owing to spin-dependent transport similar to the tunneling magnetoresistance (TMR) effect in magnetic tunnel junctions [Sugahara 2005]. However, it is predicted that the magneto-current ratio in the spin MOSFET will exhibit unwanted bias-dependence, that is, it decreases with increasing bias voltages, just like the TMR effect. Another way to realize a spin MOSFET using a ferromagnetic metal for the source and drain is to employ a tunneling junction, instead of a Shottsky junction. Possible materials for the ultrathin tunnel barrier between the ferromagnetic metal and the Si channel are SiO_2, Al_2O_3, and MgO [Dennis 2003; Van't Erve et al. 2004; Salis et al. 2005].

Figure 1(c) schematically shows the device structure of a spin MOSFET using half-metallic ferromagnet (HMF) contacts for the souce/drain. HMFs have metallic and insulating spin bands, and thus a spin polarization of 100% at the Fermi energy. The metallic spin band of the HMF contact forms a Schottky junction with the Si channel (as described later). This type of spin MOSFET can also be applied to accumulation- and inversion-type channel devices. Possible candidates for HMF materials are Heusler alloys, CrO_2, Fe_2O_3, half-metallic compounds (CrAs, MnAs, and CrSb) with zinc-blend (ZB)-type crystal structures, and FSs [de Groot et al. 1983; Yanase and Shiratori 1984; Schwarz 1986; Shirai 2001, 2003; Sato and Katayama-Yoshida 2002]. In particular, half-metallic ZB-type compounds and FSs using a wide gap semiconductor as a host material are promising, since their predicted high Curie temperature and large band gap of

the insulating spin band [Shirai et al. 2001, 2003; Sato and Katayama-Yoshida 2002] are useful for the HMF source/drain in the spin MOSFET [Sugahara and Tanaka 2004]. The operating principle and theoretically predicted device performance are described in Section 3.

Figure 1(d) schematically shows another type of spin MOSFET. The device has a MOS capacitor structure with an FS channel and an FM (or HMF) source/drain. The interfaces between the source/drain and the FS channel are Schottky junctions. Although the structure is similar to Schottky MOSFETs [Lepselter and Sze 1968; Hattori et al. 1992; Hattori and Shirafuji 1994], this type of spin MOSFET should be operated in the accumulation-channel mode. Note that it is *not* necessary to make both source and drain contacts FM (or HMF)/FS Schottky junctions. A nonmagnetic-metal/FS Schottky junction can be used for one of the source and drain contacts. Possible candidates for channel materials are group-IV(Si, Ge, and SiGe)-based FSs [Araki et al. 2002, 2003; Stroppa et al. 2003; Park et al. 2002; D'Orazio et al. 2003; Cho et al. 2002; Tsui et al. 2003; Shuto et al. 2006]. Recently, it has become well recognized that SiGe and Ge, as well as Si and strained Si, are important as channel materials for advanced MOSFETs with high performance [Takagi 2002; Takagi et al. 2005; Tezuka et al. 2005; Maeda et al. 2005]. $Si_{1-x}Mn_x$ and $Ge_{1-x}Mn_x$ are theoretically predicted to be FSs [Araki et al. 2002, 2003; Stroppa et al. 2003], and experimental investigations have been performed by several groups. The successful epitaxial growth of ferromagnetic $Ge_{1-x}Mn_x$ films and their field-effect control of ferromagnetism were demonstrated [Park et al. 2002; D'Orazio et al. 2003]. High Curie temperatures of close to room temperature were also reported for $Ge_{1-x}Mn_x$ and $Ge_{1-x-y}Mn_xCo_y$ [Cho et al. 2002; Tsui et al. 2003]. Nevertheless, the origin of their ferromagnetism is still under investigation [Li et al. 2005; Sugahara et al. 2005]. Possible materials for the source/drain are FMs with large spin-polarization and HMFs (noted earlier). This type of spin MOSFET exhibits large magneto-current which is insensitive to bias conditions [Sugahara and Tanaka 2005]. The electrical manipulation of magnetization reversal of the FS channel is also useful for nonvolatile memory applications [Sugahara and Tanaka 2005].

3. OPERATING PRINCIPLE AND DEVICE PERFORMANCE OF SPIN MOSFETs

3.1 Operating Principle

In Section 3, the operating principle and theoretically predicted device performance of the *n*-channel accumulation-type spin MOSFET using HMF contacts for the source/drain (Figure 1(c)) is described. Figure 2(a) schematically shows the band diagram of the spin MOSFET under a common source bias condition both with and without a gate-source bias V_{GS}, where the relative magnetization configuration of the HMF source/drain is parallel. Owing to the metallic and insulating spin bands of the HMF source/drain material, spin-dependent barrier structures appear as shown in the figure, that is, a Schottky barrier (SB) with a lower barrier height ϕ^{SB} for up-spin electrons and a rectangular energy barrier

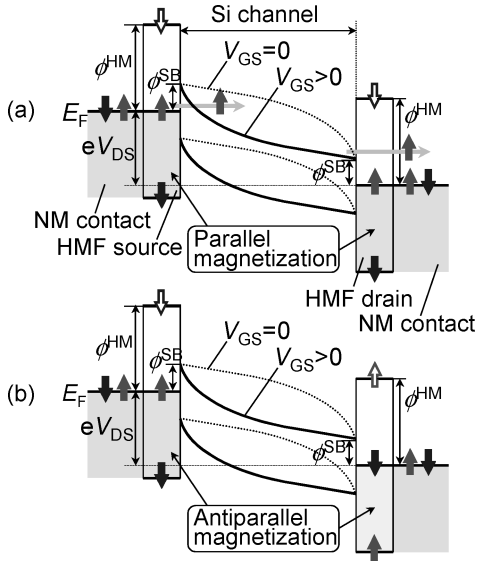

Fig. 2. Schematic band diagrams of the spin MOSFET in (a) parallel and (b) antiparallel magnetization configurations. Solid arrows in the HMF source/drain show up-spin and down-spin electrons at the Fermi energy of the metallic spin band and at the valence band edge of the insulating spin band. Open arrows represent the conduction band edge of the insulating spin band of the HMF source/drain.

with a higher barrier height ϕ^{HM} for down-spin electrons (hereafter, this spin configuration at the HMF source is used throughout this article).

When a drain-source bias V_{DS} (>0) is applied at $V_{GS} = 0$, neither up-spin nor down-spin electrons are injected from the source to the channel due to the reverse-biased source-SB for up-spin electrons (as shown by the upper dotted curve in Figure 2(a)) and the high rectangular barrier for down-spin electrons. By applying $V_{GS}(>0)$, the width of the source-SB is reduced (as shown by the upper solid curve in Figure 2(a)) and thus, up-spin electrons in the metallic spin band of the HMF source can tunnel through the thinned source-SB into the channel. On the other hand, the injection of down-spin electrons is blocked, even under the nonzero biases of V_{DS} and V_{GS}, owing to the high rectangular barrier at the source. Thus, the HMF source acts not only as a contact for blocking the off-current but also as a spin-injector of up-spin electrons from the HMF source to the channel. In the parallel magnetization configuration, the up-spin electrons injected into the channel can be transported to the nonmagnetic drain contact through the metallic up-spin band of the HMF drain, resulting in a drain current. By flipping the magnetization of the HMF drain, the antiparallel magnetization configuration is realized and the HMF barrier height for up-spin electrons becomes higher at the drain, as shown in Figure 2(b). Thus, the up-spin electrons can hardly pass through the HMF drain to the nonmagnetic drain contact. Namely, the HMF drain has the function of a spin-detector, that is, the HMF drain selectively extracts up-spin electrons from the channel when the magnetization of the HMF source and drain are parallel.

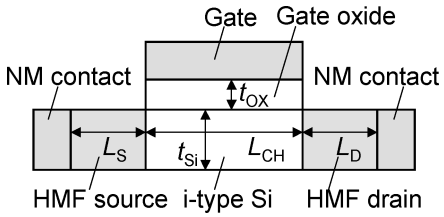

Fig. 3. Device structure used for the analysis. The size of the device in our calculation is as follows: $t_{OX} = 2.0$–3.0 nm, $t_{Si} = 10$ nm, $L_{CH} = 30$ nm, and $L_S = L_D = 5$ nm.

By combining these spin-filter effects of the HMF source/drain, an extremely large magneto-current ratio can be expected due to the high spin-selectivity of the HMF source/drain.

3.2 Theoretical Prediction of Device Performance

A model device used in our analysis is shown in Figure 3, where a thin-film-transistor structure was used for simplicity of calculation. The size of this model device is as follows: The gate oxide (SiO_2) thickness t_{OX} is 2.0–3.0 nm, the Si channel layer thickness t_{Si} is 10 nm, and the channel length L_{CH} is 30 nm. The device parameter L_S (L_D) shown in the figure is the distance from the source (drain) junction to the nonmagnetic contact. An intrinsic Si layer was used for the channel and ballistic transport was assumed for the spin-polarized electrons injected into the channel. A relatively small SB height of $\phi^{SB} = 0.2$ eV for the metallic spin band of the HMF source/drain was taken in order to achieve a large drain current. A barrier height of $\phi^{HM} = 1.0$ eV for the rectangular barrier of the HMF source/drain and a distance of $L_S = 5$ nm ($= L_D$) were selected in order to obtain a fully spin-polarized electron injection from the HMF source, as discussed later. The effective mass $m_{Si}{}^*$ of the Si layer used in the calculation was $0.19\,m_0$, where m_0 is the free electron mass, and effective masses $m_M{}^* = m_0$ and $m_I{}^* = m_{Si}{}^*$ were assumed for the metallic and insulating spin bands of the HMF source/drain, respectively. The operating temperature was set at 300 K in all the calculations. The output characteristics were calculated using the Tsu-Esaki formula [Tsu and Esaki 1973] with a two-dimensional transmission probability calculation.

In order to clarify the spin-filter effect of the HMF source, the spin injection efficiency from the source to the channel was calculated. Although the HMF source is fully polarized to up-spin (spin polarization = unity), the spin polarization of the injected electrons does not reach 100% when ϕ^{HM} or L_S is small. This is because down-spin electrons in the nonmagnetic source contact can transmit through the low or thin rectangular barrier, owing to thermionic and/or tunneling emission. Thus, a largely spin-polarized current can be obtained by increasing ϕ^{HM} and L_S. In the following calculation, we used the device parameters of $\phi^{HM} = 1.0$ eV and $L_S = 5$ nm, which are large enough for the fully spin-polarized electron injection from the source.

Solid and dashed curves in Figure 4 show the calculated output characteristics of the spin MOSFET for the parallel and antiparallel magnetization configurations, respectively, where t_{OX} is 3 nm. In the parallel magnetization,

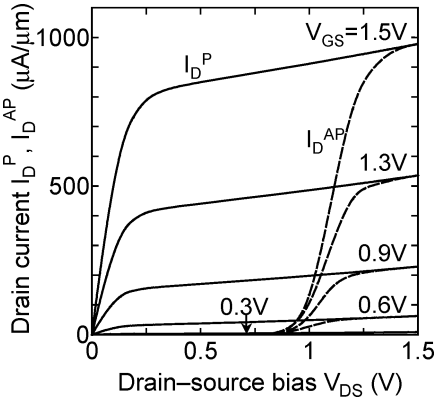

Fig. 4. Output characteristics of the spin MOSFET with $t_{OX} = 3.0$ nm. The drain currents I_D^P (solid curves) and I_D^{AP} (dashed curves) in the parallel and antiparallel magnetic configurations, respectively, are plotted as a function of V_{DS}, where V_{GS} is varied from 0.3–1.5 V.

the drain current I_D^P starts to increase at V_{GS} of more than 0.3 V (indicating the threshold voltage of 0.3 V) and increases nonlinearly with increasing V_{GS}, while I_D^P shows saturation behavior for V_{DS}. The value of I_D^P is comparable to that of sub100 nm scale MOSFETs [Iwai 1999], and I_D^P increases with decreasing the SB height (ϕ^{SB}) and gate oxide thickness (t_{OX}) like the conventional Schottky barrier MOSFETs [Hattori and Shirafuji 1994; Saito et al. 1999]. A large I_D^P of more than 1500 μA/μm can be obtained for $\phi^{SB} = 0.2$ eV and $t_{OX} =$ 2.0 nm with a gate-bias condition of $V_{GS} = 1.5$ V. Note that reduction of t_{OX} is also important to obtain the saturation behavior of I_D^P and thus, the channel conductance of the spin MOSFET (discussed later) is improved by the reduction of t_{OX}.

In the antiparallel magnetization configuration, the drain current I_D^{AP} is negligibly small for V_{DS} of less than $\phi^{HM}/e(= 1.0$ V), but I_D^{AP} increases exponentially with increasing V_{DS} and reaches the same current value as I_D^P when V_{DS} is more than $\phi^{HM}/e(= 1.0$ V), as shown in Figure 4. Thus, magnetization-configuration-dependent output characteristics are realized when $V_{DS} < \phi^{HM}/e$. The exponential increase of I_D^{AP}can be attributed to the ballistic transport in the channel region, that is, up-spin electrons injected from the HMF source can pass over the large rectangular barrier of the HMF drain when V_{DS} increases to more than $\phi^{HM}/e = 1.0$ V. Note that when the drain current is governed by drift-diffusion kinetics rather than ballistic transport, the exponential increase of I_D^{AP} is significantly suppressed. In this case, however, dynamically accumulated spin-polarized electrons in the channel would affect I_D^{AP} due to their finite spin lifetime for spin flipping.

Figure 5 shows the magneto-current ratio γ_{MC} of the spin MOSFET as a function of V_{DS} at $V_{GS} = 1.5$ V, where γ_{MC} is defined by $(I_D^P - I_D^{AP})/I_D^{AP}$, as described previously. γ_{MC} exponentially falls with increasing V_{DS}, since I_D^{AP} increases exponentially with increasing V_{DS} when V_{DS} is less than ϕ^{HM}/e, as described above. In spite of this bias-dependence, extremely large γ_{MC} of more

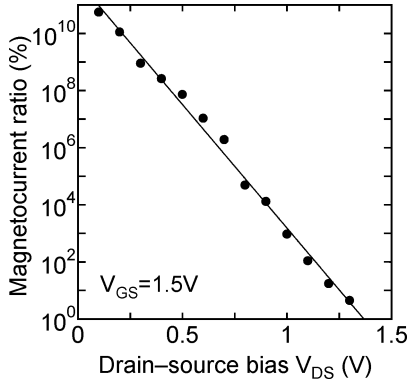

Fig. 5. Magneto-current ratio $\gamma_{\rm MC}$ [$= (I_{\rm D}^{\rm P} - I_{\rm D}^{\rm AP})/I_{\rm D}^{\rm AP}$] as a function of $V_{\rm DS}$ at $V_{\rm GS} = 1.5$ V.

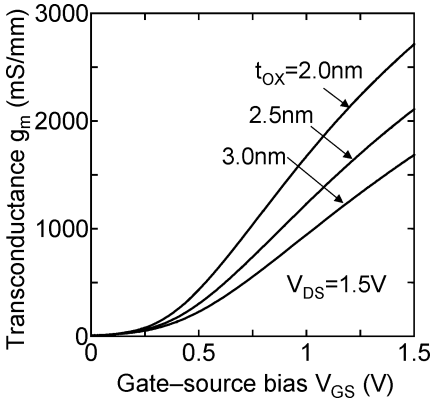

Fig. 6. Transconductance $g_{\rm m}$ ($=\partial I_{\rm D}^{\rm P}/\partial V_{\rm GS}$) as a function of $V_{\rm GS}$ at $V_{\rm DS} = 1.5$ V for $t_{\rm OX} = 2.0$, 2.5 and 3.0 nm.

than 1000 % can be obtained for $V_{\rm DS}$ less than 1.0 V. To obtain even larger $\gamma_{\rm MC}$, higher $\phi^{\rm HM}$ values are required. It should be noted that when the spin injection efficiency of the HMF source is less than unity, $\gamma_{\rm MC}$ is reduced but this strong bias-dependence of $\gamma_{\rm MC}$ is significantly suppressed (as shown in Figure 8).

The results shown in Figures 4 and 5 indicate that the spin MOSFET possesses magnetization-configuration-dependent output characteristics with large $\gamma_{\rm MC}$. Thus, the spin MOSFET satisfies the aforementioned requirement (i) for spintronic integrated circuit applications. The other requirements were examined by the on- and off-current characteristics of the spin MOSFET as follows: Figure 6 shows the transconductance $g_{\rm m}$ of the spin MOSFET in the parallel magnetization configuration as a function of $V_{\rm GS}$ at $V_{\rm DS} = 1.5$ V, where $t_{\rm OX}$ is varied from 2.0 to 3.0 nm. Here, $g_{\rm m}$ is defined by a derivative $\partial I_{\rm D}^{\rm P}/\partial V_{\rm GS}$ under a fixed $V_{\rm DS}$ condition, which is a measure of the output-current ($I_{\rm D}^{\rm P}$) drive capability of the input voltage ($V_{\rm GS}$). Since $I_{\rm D}^{\rm P}$ increases nonlinearly ($I_{\rm D}^{P} \propto F^2 exp(-1/F)$) with the increasing strength F of the electric field through the source-SB [Hattori and Shirafuji 1994], $g_{\rm m}$ increases with increasing $V_{\rm GS}$ and with decreasing $t_{\rm OX}$, as shown in Figure 6. A large $g_{\rm m}$ of 1000 mS/mm, which

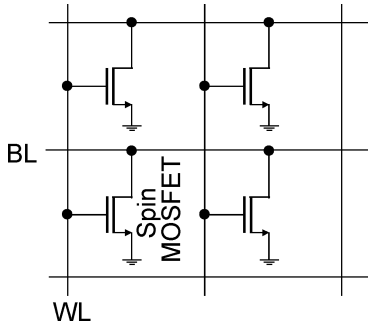

Fig. 7. Nonvolatile memory cell using a single spin MOSFET.

is comparable to (or larger than) that of sub100 nm scale MOSFETs[Iwai 1999], can be obtained at $V_{GS} = 1.0$ V for $t_{OX} = 3$ nm, and g_m is further enhanced to more than 1500 mS/mm by reducing t_{OX} to 2 nm, as shown in the figure. These large g_m values of the spin MOSFET lead to a small propagation delay t_{pd} and a large voltage gain G_V, since t_{pd} and G_V can be estimated by C_L/g_m and g_m/g_D, respectively, where C_L is a load capacitance including a parasitic capacitance and g_D is a channel conductance given by $\partial I_D^P/\partial V_{DS}$.

Furthermore, the large g_m of the spin MOSFET enables low-voltage operation, and the voltage swing could be less than 1.0 V. This results in a small power-delay product $P \cdot t_{pd}$ (that corresponds to the energy per switching) since this energy is proportional to the square of the voltage swing [Cooper 1981]. The power dissipation is also caused by the off-current in the stand-by condition of the spin MOSFET, which is characterized by the subthreshold swing S calculated from $\log I_D^P - V_{GS}$ characteristics. Although S depends on device parameters such as t_{OX}, t_{Si}, L_{Si}, and ϕ^{SB}, S can take <100 mV/decade, implying a relatively small off-current [Sugahara 2005].

From our predictions, the spin MOSFET presented here [Sugahara and Tanaka 2004] and the other types of spin MOSFETs [Sugahara 2005; Sugahara and Tanaka 2005] are expected to show the excellent performance in the sub100 nm regime and they have a simple device structure, as shown in Figure 1. Thus, we can expect the scaling merits by downsizing the spin MOSFETs and the high degree of integration. Therefore, the spin MOSFETs potentially satisfy all the requirements (i)–(v) for spin-electronic integrated circuit applications.

4. NOVEL INTEGRATED CIRCUIT ARCHITECTURES EMPLOYING SPIN MOSFETs

4.1 Nonvolatile Memory

Figure 7 schematically shows nonvolatile memory cells using a spin MOSFET. A core (storage array) is made up of a single spin MOSFET. Thus, the cell size can ultimately be small, leading to an extremely high degree of device integration. Each cell shares a gate connection (wordline; WL) with the other cells in the same column, and a drain connection (bitline; BL) is shared by the cells in the same row. Thus, memory addresses can be accessed in random order. Each

cell (spin MOSFET) can store one bit of binary information via the parallel or antiparallel magnetization of the spin MOSFET. The readout operation is performed by applying a bias to the selected cell. In particular, precharging the bitline could be the most promising way to conduct the readout operation, as in the case of flash memory and dynamic random access memory. The amount of the drain current is interpreted as stored information, that is, large and small drain currents correspond to the currents in the parallel and antiparallel magnetizations, respectively. A fast readout time and excellent fault tolerance in the readout operation can be expected for the spin MOSFET memory cells due to the useful features of the spin MOSFETs, such as extremely large magneto-current (in the case of the spin MOSFET shown in Figure 1(c)) [Sugahara and Tanaka 2004], very large output current (in the case of Figure 1(b)) [Sugahara 2005], or bias-independent large magneto-current (in the case of Figure 1(d)) [Sugahara and Tanaka 2005]. For the writing operation, the magnetization configuration of the spin MOSFET is changed by a magnetic field induced by currents through the interconnections in the integrated circuit. This writing operation is equivalent to that of other nonvolatile memory (MRAM) [Daughton 1997; Inomata 2001; Tehrani et al. 2003; Katti 2003] using two-terminal magnetoresistive devices as memory elements.

When a spin MOSFET is used in an ultrahigh-density memory cell, one of the important challenges is magnetization reversal. This is because the current required for magnetization reversal increases when decreasing the device size to a nanoscale dimension, owing to the large demagnetizing field of a nanoscale ferromagnet. This will lead to a fatal increase of power dissipation and programming disturbs [Tehrani et al. 2003] that is a common problem for MRAM and spin MOSFET-based nonvolatile memory (the failure mechanism referred to as a "programming disturb" is due to a stray magnetic field from selected interconnections (word and bit lines) of programming to unselected spin MOSFETs that are connected to one of the selected interconnections). Recently, current-induced magnetization reversal (CIMR) via spin transfer torque attracts much interest as a scalable means of magnetization reversal in two-terminal magnetoresistive devices such as spin valves and magnetic tunnel junctions [Slonczewski 1996; Albert et al. 2000; Jiang et al. 2004; Fuchs et al. 2004; Moriya et al. 2004; Chiba et al. 2004]. In the writing scheme using CIMR, magnetization reversal can be performed by the injection of a spin-polarized current into a ferromagnetic layer, since the spin-polarized current exerts torque for magnetization reversal in the ferromagnetic layer. Since the source/channel/drain structure of the spin MOSFET is considered to be a kind of spin valve or magnetic tunnel junction when the channel length is shorter than the spin relaxation length, the writing scheme using CIMR is also applied to spin MOSFETs with a ferromagnetic semiconductor (FS), ferromagnetic metal (FM), or half-metallic ferromagnet (HMF) for the ferromagnetic source/drain (Figure 1(a)–(c)). Although a relatively large current density is required for CIMR, the spin MOSFETs can drive such high current density due to their high transconductance [Sugahara and Tanaka 2004; Sugahara 2005; Sugahara and Tanaka 2005]. Note that the current density for CIMR can be drastically reduced by using a material that has a small saturation magnetization. In this sense, the spin MOSFET with the FS

source/drain (Figure 1(a)) is promising to reduce the current density required for CIMR, since the saturation magnetization of FSs is typically smaller than that of ferromagnetic transition metals by two orders of magnitude. It should be also noted that CIMR is highly effective to eliminate programming disturbs.

The electrical manipulation of magnetization reversal (EMMR) [Ohno et al. 2000; Chiba et al. 2003] will be an promising alternative way to realize magnetization reversal for the spin MOSFET with the FS channel (Figure 1(d)). Because of the carrier-mediated ferromagnetism in FS, the ferromagnetic-paramagnetic phase transition can be controlled by the carrier density of the FS channel, that is, when the carrier density of the FS channel is reduced by applying a gate electric field through a metal/insulator/FS structure, the ferromagnetic ordering can be changed to a paramagnetic character. The magnetization reversal of the paramagnet can be easily accomplished by a very small magnetic field (much less than the coercivity of the FS), and the ferromagnetic ordering is recovered by removing the application of the gate electric field. Although this writing scheme is similar to the Curie point writing in magneto-optical recording and to the recently proposed writing process using resistive heating in MRAM [Daughton and Pohm 2003; Prejbeanu et al. 2004], it is obviously suitable for integrated circuit applications to use EMMR in which the phase transition of an FS can be obtained by the application of an electric field, rather than laser irradiation heating or resistive heating in the Curie point writing. A very low writing power and excellent fault tolerance for programming can be expected for the spin MOSFET cell with the EMMR writing scheme. Detailed nonvolatile memory architecture based on EMMR with a spin MOSFET has been described elsewhere [Sugahara and Tanaka 2005].

4.2 Reconfigurable Logic

The reconfigurable logic gates shown in this subsection can be designed by combining spin MOSFETs with a neuron MOS (νMOS) input stage. As described above, spin MOSFETs have high transconductance ($g_{\mathrm{m}}^{\mathrm{P}}$) in the parallel magnetization configuration and low transconductance ($g_{\mathrm{m}}^{\mathrm{AP}}$) in the antiparallel magnetization configuration. While a large $g_{\mathrm{m}}^{\mathrm{P}}$ and a negligibly small $g_{\mathrm{m}}^{\mathrm{AP}}$ are favorable for nonvolatile memory applications, a large $g_{\mathrm{m}}^{\mathrm{P}}$ and a moderate $g_{\mathrm{m}}^{\mathrm{AP}}$ are required for reconfigurable logic applications. Both the spin MOSFET with the HMF source/drain (Figure 1(c)) and the spin MOSFET with the FS channel (Figure 1(d)) are expected to show ideal output characteristics for reconfigurable logic applications. Figure 8 shows the calculated output characteristics of a spin MOSFET with the HMF source/drain, where the distance L_{S} (shown in Figure 3) of the HMF source is only 0.5 nm (shorter than the $L_{\mathrm{S}} = 5$ nm which is used in the calculation of Figure 4) so that the spin injection efficiency from the source to the channel is reduced and therefore, the minority-spin electrons of the HMF source can be injected from the nonmagnetic contact to the channel through the energy barrier caused by the insulating spin band of the HMF source. Although $I_{\mathrm{D}}^{\mathrm{AP}}$ is smaller than $I_{\mathrm{D}}^{\mathrm{P}}$ for a V_{DS} less than ϕ^{HM}/e ($= 1$V), $I_{\mathrm{D}}^{\mathrm{AP}}$ is not negligibly small, but a moderate amount of $I_{\mathrm{D}}^{\mathrm{AP}}$ is obtained in Figure 8 owing to the transport of minority-spin electrons in the antiparallel

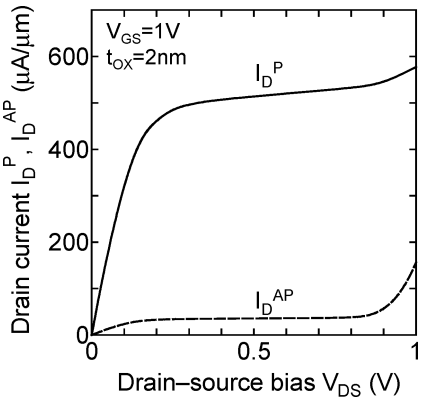

Fig. 8. Output characteristics of the spin MOSFET for reconfigurable logic gates, where $t_{OX} = 2.0$ nm, $t_{Si} = 10$ nm, $L_{CH} = 30$ nm, $L_S = 0.5$ nm, and $L_D = 5$ nm. The drain currents I_D^P (solid curves) and I_D^{AP} (dashed curves) in the parallel and antiparallel magnetic configurations, respectively, are plotted as a function of V_{DS}, where V_{GS} is fixed at 1.0 V.

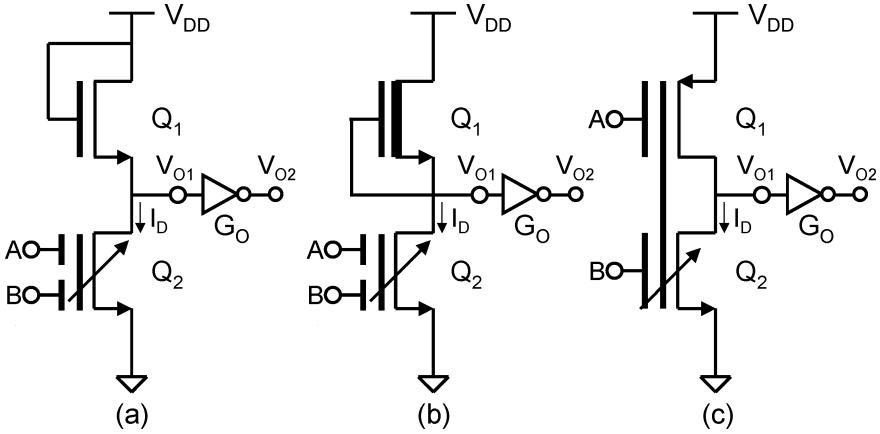

Fig. 9. Reconfigurable NAND/NOR gates using a spin MOSFET with (a) E/E, (b) E/D, and (c) CMOS configurations. Q_1 (ordinary MOSFET) is the active load and Q_2 (spin MOSFET) is the driver.

magnetization configuration. On the contrary, the drain current I_D^{AP} is negligibly small in the antiparallel magnetization configuration when L_S is significantly large ($L_S = 5$ nm), as described in Figure 4.

Figure 9 shows reconfigurable AND/OR gates employing a spin MOSFET where the spin MOSFET acts as the driver (Q_2) of (a) E/E, (b) E/D, and (c) CMOS inverters with a νMOS input stage having two binary inputs (A and B). It should be noted that the reconfigurable AND/OR gates can also be constructed by using a spin MOSFET as the active load (Q_1). Although the logic gates shown in Figure 9 can act as NAND/NOR gates for the output V_{O1}, the inverter G_O at the output stage should be used for the inverse amplification of the output from V_{O1} to V_{O2} to restore the degraded logic swing of V_{O1}, as described later. Since the logic functions for the output V_{O2} are easily obtained from the inverted

logic functions for the output V_{O1}, the operation of the reconfigurable logic gate is described here for the output V_{O1}, concentrating on the reconfigurable NAND/NOR CMOS gate (Figure 9(c)).

The reconfigurable NAND/NOR CMOS gate can be realized by using a p-channel ordinary MOSFET as the active load (Q_1) and an n-channel spin MOSFET as the driver (Q_2) of a CMOS inverter with a νMOS input stage, as shown in Figure 1(c). Note that this logic gate can also be configured with a p-channel spin MOSFET as Q_1 and an n-channel MOSFET as Q_2, and with p- and n-channel spin MOSFETs as Q_1 and Q_2, respectively. The νMOS input stage consists of a floating gate coupled capacitively with two input gates. The floating-gate voltage V_{FG} of the νMOS is given by[Shibata and Ohmi 1992, 1993]:

$$V_{FG} = \frac{C_A A + C_B B}{C_0 + C_A + C_B} = \frac{A + B}{2}, \tag{1}$$

where C_0 denotes a capacitance between the substrate and the floating gate, C_A and C_B represent a coupling capacitance for inputs A and B, and we assume $C_A = C_B$ and C_A,$C_B \gg C_0$. The binary input voltages of 0 and V_{DD} for A and B can be simply expressed by "0" and "1" which are measured in units of V_{DD} (hereafter, quotation marks are used to denote values measured in units of V_{DD}). When the input combinations are (A, B) = ("0", "0") and (A, B) = ("1", "1"), V_{FG} is "0" and "1," respectively. When one of the two inputs is "1," that is, (A, B) = ("1", "0") or ("0", "1"), V_{FG} is "1/2."

Figure 10 shows the load line diagrams of the reconfigurable NAND/NOR CMOS gate for the output V_{O1} (the output inverter G_O is not included). Bold and thin solid curves in Figures 10(a)–(c) show the output characteristics of the driver spin MOSFET Q_2 in the parallel and antiparallel magnetization configurations, respectively, and dashed curves show the output characteristics of the load MOSFET Q_1. The load line diagrams (a)–(c) correspond to the cases at V_{FG}="0," "1/2," and "1," respectively. Operating points determining the output voltage of this reconfigurable logic gate are given by the intersection between the load and driver curves. When (A, B) = ("0," "0"), the driver spin MOSFET Q_2 is in the off-state due to V_{FG} = "0," as shown in Figure 10(a). Thus, the operating point is P_1 shown in the figure that gives the output voltage of "1". When (A, B) = ("1," "1"), the load MOSFET Q_1 is in the off-state due to V_{FG} = "1," as shown in Figure 10(c). Thus, the operating point becomes P_2 corresponding to the output voltage of "0." These logic functions do not depend on the magnetization configuration of the spin MOSFET Q_2 because one of the driver and load transistors is in the off-state. When (A, B) = ("1," "0") or ("0," "1"), both Q_1 and Q_2 are in the on-state (see Figure 10(b)). The saturation currents I_1, I_2^{P}, and I_2^{AP} of Q_1 and Q_2 in the parallel and antiparallel magnetization configurations, respectively, are designed to satisfy the relation $I_2^{AP} < I_1 < I_2^{P}$, as described later. In the parallel magnetization configuration, the operating point is P_3 near the output voltage of "0" (denoted as "$\sim$0" in Figure 10(b)). In the antiparallel magnetization configuration, the operating point is P_4 near the output voltage of "1" (denoted as "$\sim$1" in Figure 10(b)). In the case of (A, B) = ("1," "0") or ("0," "1"), the output V_{O1} shows deviations from the complete "0" and "1" states.

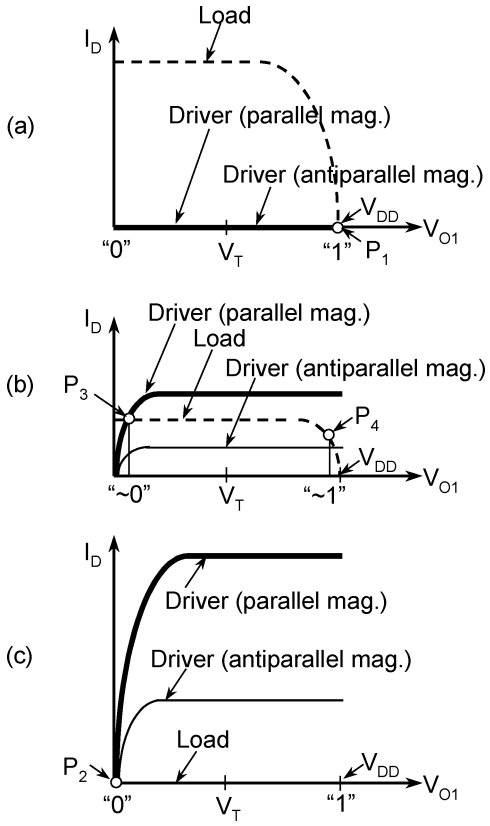

Fig. 10. Lad-line diagram of the reconfigurable NAND/NOR CMOS gate (Figure 9c) for (a) (A, B) = ("0," "0"), (b) (A, B) = ("0," "1"), and (c) (A, B) = ("1," "1").

Table I. Truth Table of the Reconfigurable Circuit of Figure 9c, Where P and AP Represent the Parallel and Antiparallel Magnetization Configurations, Respectively

			P		AP	
A	B	V_{FG}	V_{O1}	V_{O2}	V_{O1}	V_{O2}
0	0	0	1	0	1	0
0	1	1/2	~0	1	~1	0
1	0	1/2	~0	1	~1	0
1	1	1	0	1	0	1

However, these deviations can be included in the logic margin, that is, using the logic margin ΔV, the "0" level for V_{O1} means "0" $\leq V_{O1} \leq$ "0"$+\Delta V$, and the "1" level for V_{O1} "1"$-\Delta V \leq V_{O1} \leq$ "1." These deviations can be eliminated using the output inverter G_O, although the logic functions are inverted. The results are summarized in Table I. NOR (OR) and NAND (AND) logic can be realized for the output V_{O1} (V_{O2}) in the parallel and antiparallel magnetization configurations, respectively.

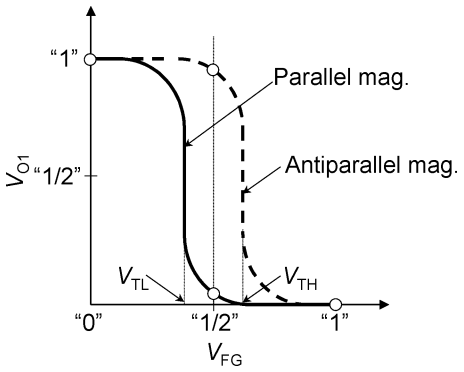

Fig. 11. Schematic transfer characteristics (V_{FG} vs. V_{O1}) with Q_2 in the parallel magnetization configuration (solid curve) and in the antiparallel magnetization configuration (dashed curve).

By applying a simple MOSFET model to a spin MOSFET, the transfer characteristics (input voltage vs. output voltage) of the reconfigurable NAND/NOR gate can be easily analyzed. The simple MOSFET model given by the gradual channel approximation seems to be useful for the spin MOSFET [Matsuno et al. 2004]. To reproduce the magnetization-configuration-dependent output characteristics of the spin MOSFET, large and small gain coefficients are introduced into the device model of a single spin MOSFET, that is, the spin MOSFET in parallel (antiparallel) magnetization is represented by a MOSFET with a large (small) gain coefficient β^{P} (β^{AP})[1]. These bias-independent parameters are quite useful for the operation analysis of the logic gate. In the following part of this section, semiquantitative analysis using gain coefficients are described for the reconfigurable NAND/NOR CMOS gate shown in Figure 9(c). The gain coefficients of Q_1 and Q_2 in parallel and antiparallel magnetization configurations are expressed by β_1, β_2^{P}, and β_2^{AP}, respectively, and these are set to satisfy $\beta_2^{AP} < \beta_1 < \beta_2^{P}$,which is required for the reconfigurable NAND/NOR function, as shown in Figure 10. Solid and dashed curves in Figure 11 schematically show the transfer characteristics (V_{O1} vs. V_{FG}) of the reconfigurable logic gate in parallel and antiparallel magnetizations for the spin MOSFET Q_2. This transfer characteristic can be easily obtained by using the load line diagrams shown in Figure 10. The logic threshold voltage V_T of the reconfigurable logic gate is given by

$$V_T = \frac{V_{DD} - |V_{t1}| + V_{t2}\sqrt{\beta_2{}^{\zeta}/\beta_1}}{1 + \sqrt{\beta_2{}^{\zeta}/\beta_1}}, \tag{2}$$

where V_{t1} and V_{t2} are the threshold voltages for the drain currents of Q_1 and Q_2, respectively, and ζ is denoted P for parallel magnetization and AP for antiparallel magnetization. When $|V_{t1}| \approx V_{t2}$, V_T is lower than "1/2" for $\beta_2^{\zeta}/\beta_1 > 1$ and is higher than "1/2" for $\beta_2^{\zeta}/\beta_1 < 1$. Namely, when the magnetization of

[1]In the gradual channel approximation model of MOSFETs, the gain coefficient β is given by $\beta = I_{Dsat}/(V_{GS} - V_t)^2$, where I_{Dsat}, V_{GS}, and V_t are the saturation drain current, the gate-bias, and the threshold voltage of the drain current, respectively.

the source and drain of Q_2 is parallel, the logic threshold voltage V_T is V_{TL}, which is lower than "1/2." By flipping the magnetization of Q_2 from the parallel to the antiparallel configuration, the logic threshold voltage V_T is changed to V_{TH}, which is higher than "1/2."

The logic operations of the reconfigurable NAND/NOR gate can be obtained using the transfer characteristics shown in Figure 11. When the spin MOSFET Q_2 is in the parallel magnetization configuratuin, the logic threshold voltage V_{TL} is lower than "1/2," as shown by the solid curve in the figure. For the input combinations of (A, B) = ("0," "0"), [("1," "0") or ("0," "1")], and ("1," "1"), V_{FG} takes "0," "1/2," and "1," respectively, as described previously. These V_{FG} values are transformed to V_{O1} = "1," "0," and "0," respectively, via the transfer characteristics. Thus, the reconfigurable logic gate shows a NOR function when Q_2 is in the parallel magnetization configuration. Note that when V_{FG} = "1/2" [(A, B) = ("1," "0") or ("0," "1")], V_{O1} is slightly higher than "0." However, this deviation can be included in the logic margin, as described above. This deviation disappears after the inverse amplification from V_{O1} to V_{O2} by the output inverter G_O, while the logic function is inverted from NOR for the output V_{O1} to OR for V_{O2}.

When the spin MOSFET Q_2 is in antiparallel magnetization, the logic threshold voltage V_{TH} is higher than V_{FG} = "1/2," as shown by the dashed curve in Figure 2(b). Owing to this transfer characteristic, the input combinations of (A, B) = ("0," "0"), [("1," "0") or ("0," "1")], and ("1," "1") (corresponding to V_{FG} = "0," "1/2," and "1," respectively) are transformed to V_{O1} = "1," "1," and "0." Thus, the reconfigurable logic gate shows a NAND function when Q_2 is in the antiparallel magnetization state. Note that when V_{FG} = "1/2" " [(A, B) = ("1," "0") or ("0," "1")], V_{O1} is slightly lower than "1." This deviation can be eliminated by the output inverter G_O. The logic function for the output V_{O2} is inverted from NAND to AND.

It should be noted that the operational margin ($V_{TH}-V_{TL}$) depends on the ratio β^P/β^{AP}. The appropriate range of β^P/β^{AP} seems to be extremely wide from our circuit simulation results using a simple device model of the spin MOSFET [Matsuno et al. 2004]. Also, note that the operating speed and power dissipation of the proposed reconfigurable logic gates depend on the gain coefficient ratio β^P/β^{AP}, that is, a large β^P/β^{AP} ratio results in small power dissipation at the expense of the operating speed.

A variety of reconfigurable logic functions can be designed by adding a small number of spin MOSFETs and conventional MOSFETs to this NAND/NOR gate. The reconfigurable symmetric Boolean functions (AND, OR, XOR, NAND, NOR, XNOR, All-"0" and All-"1") for two-input variables can be realized by only ten transistors including four spin MOSFETs. Figure 12 shows a reconfigurable logic gate for all symmetric Boolean functions (AND, OR, XOR, NAND, NOR, XNOR, All-"1," All-"0") [Matsuno et al. 2004]. A νMOS input stage and a CMOS inverter G_{12} consisting of p-channel and n-channel spin MOSFETs Q_1 and Q_2 act as a NAND/NOR gate for the output V_{O1}. A CMOS inverter G_P (G_N) and a p-channel (n-channel) spin MOSFET Q_3 (Q_4) are connected between the floating gate and the output V_{O1} terminal, as shown in Figure 12. A CMOS inverter G_O at the output stage is used for the inverse amplification of the V_{O1} signal in order

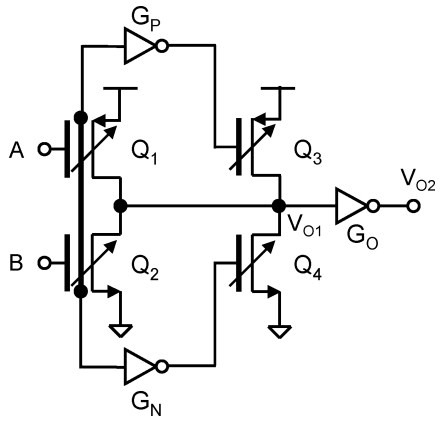

Fig. 12. Circuit configuration of a reconfigurable logic gate for two-input all symmetric Boolean functions.

Table II. Truth Table of the Reconfigurable Circuit of Figure 12 for (a) $\{Q_1, Q_2, Q_3, Q_4\} = \{\zeta_1, \zeta_2, AP, AP\}$, (b) $\{\zeta_1, \zeta_2, P, AP\}$, (c) $\{\zeta_1, \zeta_2, AP, P\}$, and (d) $\{\zeta_1, \zeta_2, P, P\}$

(a) $\{\zeta_1, \zeta_2, AP, AP\}$

$\{\zeta_1, \zeta_2\}$		{P, AP}	{AP, P}
A	B	V_{O2}	V_{O2}
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

(b) $\{\zeta_1, \zeta_2, P, AP\}$

$\{\zeta_1, \zeta_2\}$		{P, AP}	{AP, P}
A	B	V_{O2}	V_{O2}
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	1

(c) $\{\zeta_1, \zeta_2, AP, P\}$

$\{\zeta_1, \zeta_2\}$		{P, AP}	{AP, P}
A	B	V_{O2}	V_{O2}
0	0	1	1
0	1	0	1
1	0	0	1
1	1	1	1

(d) $\{\zeta_1, \zeta_2, P, P\}$

$\{\zeta_1, \zeta_2\}$		{P, AP}	{AP, P}
A	B	V_{O2}	V_{O2}
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

to eliminate deviations of V_{O1} from the complete "0" and "1" states. Note that since the *p*-channel and *n*-channel spin MOSFETs Q_3 and Q_4 can also form a CMOS configuration (G_{34}), this logic gate is compatible with CMOS technology. The logic functions of the reconfigurable logic gate can be switched by changing the combination of magnetization configurations of the spin MOSFETs Q_1, Q_2, Q_3, and Q_4. Table II shows the truth tables of this reconfigurable logic gate, where the magnetization configurations of Q_1, Q_2, Q_3, and Q_4 are specified using the expression $\{Q_1, Q_2, Q_3, Q_4\} = \{\zeta_1, \zeta_2, \zeta_3, \zeta_4\}$, and ζ_i ($i = 1, 2, 3,$ and 4) represents the magnetization configuration of Q_i and $\zeta_i = P$ (AP) is for the parallel (antiparallel) magnetization. The detailed operation analysis and numerical simulation of this reconfigurable logic gate have been described elsewhere [Matsuno et al. 2004].

A possible application of the proposed reconfigurable logic gates is in the recently emerging field programmable gate array (FPGA) [Trimberger et al.

1993; Hauck et al. 1998]. This new class of reconfigurable logic gates could be also used for reconfigurable computing, which is a new computing paradigm satisfying both flexibility and performance [Bondalapati and Prasanna 2002].

5. SUMMARY

We have reviewed the theoretically predicted device performance of recently proposed MOSFET-type spin transistors, spin MOSFETs, and their integrated circuit applications. The spin MOSFETs can exhibit significant magnetization-dependent output characteristics without sacrificing their "transistor" performance that arises from their original construction (MOSFET structure). Since Si MOS technology is the key to ultralarge-scale integration of high-density memory and high performance logic, excellent compatibility with Si MOS technology and the virtually same scalability as ordinary MOSFETs are essential advantages of spin MOSFETs. These features make the spin MOSFETs ideal spin transistors with high performance for device integration. We believe that spin MOSFETs open the door to a new development direction of semiconductor integrated electronics employing spin degree of freedom. Nonvolatile memory and reconfigurable logic architectures employing spin MOSFETs may be promising paths for spin-electronic integrated circuits.

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