Read/write operation of spin-based MOSFET using highly spin-polarized ferromagnet/MgO tunnel barrier for reconfigurable logic devices

Takao Marukame, Tomoaki Inokuchi, Mizue Ishikawa, Hideyuki Sugiyama and Yoshiaki Saito

Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corp., 1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan, Tel: +81-44-549-2075, Fax: +81-44-520-1257, E-mail: takao.marukame@toshiba.co.jp

Abstract

For future high-performance reconfigurable logic devices, we developed a novel spin-based MOSFET; "Spin-Transfer-Torque-Switching MOSFET (*STS*-MOSFET)" that enables the read/write performance and memorization of the configuration with nonvolatility by using the ferromagnetic electrodes and the spin-polarized current through Si channel and spin-transfer torque switching in magnetic tunnel junctions (MTJs) on the source/drain. The read/write operation of the *STS*-MOSFET was first demonstrated in this work. The highly spin-polarized ferromagnet/MgO tunnel barrier electrodes and the MTJs using their structure for the source/drain showed great possibility to realize our proposed *STS*-MOSFET and to enhance their performance.

Introduction

Spintronic devices have attracted much attention as promising candidates of beyond CMOS device [1]. Several types of Si-based spintronic devices such as a lateral spin valve etc. have been proposed [2, 3]. Among them, spin MOSFET have good compatibility with existing LSI [4] and have possible application of reconfigurable logic circuit such as field programmable gate array (FPGA). To realize spin MOSFET, it is essential to develop spin generation, injection into semiconductor, transportation and their detection. Spin injection and the diffusive transport in Si was demonstrated by using Fe/AlO_x electrodes and a ''non-local'' measurement [5]. We also have reported a non-local measurement in a GaAs channel using CoFeB/MgO/GaAs junctions [6]. However, up to now, obvious data of spin dependent local-transport have not been reported due to the huge contact resistances R_c. Reducing R_c at source/drain interfaces in MOSFETs is still the difficult challenge from the point of view of further scaling [7]. To obtain spin dependent local-transport in a Si channel, low R_c of ferromagnetic metal (FM)/Si are inevitable because the resistance should be in a specific range depending on the spin diffusion length in a semiconductor channel [8].

In this paper, we first report on the spin dependent local-transport though a lateral Si channel for spin MOSFET (Fig. 1). FPGA using spin MOSFET in Fig. 2 does not need to load configuration data when the power is turned on. This can dramatically reduces the number of MOS devices and the power consumption compared with the conventional FPGA. In order to operate writing FM by spin-transfer torque switching (STS), we have proposed spin-based MOSFET with magnetic tunnel junctions (MTJs); "Spin-transfer-Torque-Switching MOSFET: *STS*-MOSFET" (Fig. 1) [9]. On the other hand, Heusler alloy with potentially half-metallic ferromagnet nature and MgO tunnel barrier are desirable materials for read/write operation in spin-based MOSFET (Fig. 1(b), (c)) [10]. In this work, we first demonstrate read/write operation of *STS*-MOSFET using highly spin-polarized FM electrodes on Si substrate.

Experimental methods

The spin injection devices and MOSFETs with MTJs were fabricated on Si(001) and SOI substrates. We used a heavily doped n-type Si surface (n^+ Si) under the FM/tunnel barrier (*I*) electrodes to reduce interfacial resistance. The regions for n-type channels and n^+ Si were formed in the Si substrate by using ion implantation and annealing. The doping densities N_d in the n-Si channel layer were from ~5×10^{17} to ~5×10^{19} cm^{-3} (n^+ Si: ~5×10^{20} cm^{-3}). A tunnel barrier (MgO, SiO_x or MgO/SiO_x) was formed on the Si surface and followed by deposition of a ferromagnetic layer in an UHV sputtering system. The SiO_x layers were formed *in-situ* by radical oxidation methods in the chamber. The FM and MgO layers were deposited by magnetron sputtering (Fig. 3).

The junctions were microfabricated by photolithography, Ar ion milling and reactive ion etching. Current-voltage (*I-V*) measurements, non-local signal measurements and magnetoresistance (MR) measurements were carried out for spin injection device. Read/write operations were investigated for the bottom-gate type *STS*-MOSFET fabricated on SOI substrates.

Results and Discussion

1. Junction resistances of FM/I/Si structures

In order to obtain low junction resistance, FM/I/Si junctions were fabricated on Si substrate (Fig. 4(a)). Figure 4(b) shows resistance area products (*RA*) of FM/SiO_x/Si structures fabricated by using radical oxidation. In the junctions on a low N_d substrate, the tunnel current was low because of the wider width of the Si depletion layer (Fig. 5(a)). The obtained result indicates the tunnel conductance was strongly dependent on doping level of Si surface, showing low resistances for the junctions on n^+ Si. Figure 5(b) shows *RA* as a function of N_d with various FM/I/Si structures. These FM/I (MgO, SiO_x or MgO/SiO_x)/Si junctions had *RA* values with the wide range from 36 to 38k $\Omega\mu m^2$. We obtained relatively low *RA* of 36 $\Omega\mu m^2$ for the junctions on the n^+ Si layer.

2. Spin injection and detection through Si channel

We investigated spin transport in the Si channel by a non-local method. Here, we focus on the results obtained with CoFeB/MgO/SiO_x electrodes in the Si channel (same as shown in Fig. 6). Figure 7(a) shows the non-local voltage

difference $\Delta V_{\text{non-local}}$ at 12 K. As illustrated in Fig. 7(b), while the constant current was applied between a CoFeB/MgO/SiO_x (FM1) electrode and a non-magnetic Ti/Au contact (NM1) on Si, the $\Delta V_{\text{non-local}}$ was measured between the other contacts (FM2 and NM2). We observed the clear change of $\Delta V_{\text{non-local}}$, corresponding to the relative magnetization directions between FM1 and FM2, under the external magnetic field. The obtained result obviously shows spin transport through 1-μm-length Si channel (N_d: ~5×10^{18} cm^{-3}) from the CoFeB/MgO/SiO_x electrodes.

3. Fabrication of highly spin-polarized $Co_2Fe(Al,Si)$ films and spin dependent transport in a Si channel

Full-Heusler alloy, $Co_2Fe(Al_{0.5},Si_{0.5})$ (CFAS), features theoretically predicted high spin polarizations for both the ordered $L2_1$ structure and the disordered B2 one. Fabricated CFAS films on the substrates of MgO and MgO-buffered Si were $L2_1$ structure and B2 one, respectively (Fig. 8). From TEM observations, we confirmed the growth of highly (001)-oriented thin MgO layer on the Si substrate (Fig. 9). Figure 10 shows a high tunnel magnetoresistance (TMR) ratio of 223% for CoFeB/MgO/CFAS on a Si substrate. The CFAS/MgO/CFAS MTJs on an MgO-buffered Si substrate also shows TMR ratios up to about 120% (Fig. 11). We thus investigated non-local measurements in a Si channel using the CFAS/MgO/Si junctions. We observed clear changes of $\Delta V_{\text{non-local}}$ at 12 K, corresponding to the relative magnetization directions between FM1 and FM2 (Fig. 12). This result directly shows spin transport through Si channel from the CFAS/MgO electrodes. Furthermore, we observed an exponential dependence of $\Delta V_{\text{non-local}}$ on Si channel length L (Fig. 13). By using a fitting curve to the data, we estimated a spin diffusion length λ of 10.5 μm in the Si-channel. The obtained λ is sufficiently longer than gate lengths of state-of-the-art MOSFETs. It should be noted that a local-MR with the current path of CFAS/MgO/Si channel/MgO/CFAS and the MR ratio of about 10% at 12 K were observed in Si channel length of L = 10 μm (Fig. 14).

4. Demonstration of read/write operation of STS-MOSFET

A bottom-gate type *STS*-MOSFET was fabricated as sketched in Fig.15. The MTJ structure was CoFeB/MgO 0.85 nm/CFAS on a top-Si layer with SiO_x (Fig. 16). Figure 17 shows a cross sectional TEM image of the fabricated *STS*-MOSFET. In the device structure, we can observe MR due to spin dependent local-transport along with TMR of MTJs. Figure 18 shows I_{ds}-V_{ds} characteristics under the various V_g. The device exhibited clear change of R_{ds}-V_{ds} characteristics depending on relative magnetization directions of the two FM (Fig. 19). This demonstrates I_{on} modulation with nonvolatility originated from ferromagnetic nature of spin-based MOSFETs, which is hopeful for novel reconfigurable logic circuits. As shown in Fig. 20, the MTJ showed clear MR curves vs. magnetic field applied along the magnetization easy axis (H_{easy}). In Fig. 21, the STS effect of the MTJ occurred in the MOSFET under V_g = 5 V. The critical current for magnetization switching was decreased by the bias field of hard axis [11, 12]. We first confirmed good reproducibility of read/write operation, i.e., resistance changes by STS during 30,000 cycle test (Fig. 22) in the spin-based MOSFET.

Conclusion

For constructing novel spin-based MOSFETs, we established fabrication techniques of low *RA* for FM/I/Si junctions and highly spin-polarized Heusler alloy CFAS films on Si. Using the CoFeB/MgO/SiO_x and CFAS/MgO electrodes, we observed spin transport through Si and the MR ratio, indicating a great potential of the spin MOSFET as a key device to produce novel reconfigurable logic devices.

Moreover, read/write operation of Spin-transfer-Torque-Switching (*STS*) MOSFET using magnetic tunnel junctions for source/drain electrodes was first demonstrated in this work.

Acknowledgements

This work is partly supported by the New Energy and Industrial Technology Development Organization (NEDO).

References

[1] ITRS2007: http://www.itrs.net/Links/2007ITRS/Home2007.htm
[2] G. A. Prinz, Phys. Today, 48 (1995) 58, Science, 282 (1998) 1660.
[3] S. Datta and B. Das, Appl. Phys. Lett., 56 (1990) 665.
[4] S. Sugahara and M. Tanaka, ACM Trans. on Storage 2 (2006) 197.
[5] O. M. J. van't Erve *et al*., Applied Physics Lett. 91 (2007) 212109.
[6] T. Inokuchi *et al.*, Applied Physics Express 2 (2009) 023006.
[7] T. Marukame *et al.*, IEDM 2008, p.547.
[8] A. Fert and H. Jaffrès, Phys. Rev. B 64 (2001) 184420.
[9] Y. Saito *et al.*, USP 7411235, USP 7200037
[10] T. Marukame *et al*., Appl. Phys. Lett. 90 (2007) 012508.
[11] T. Inokuchi *et al.*, Appl. Phys. Lett. 89 (2006) 1025032.
[12] Y. Saito *et al.*, Eur. Phys. J. B59 (2007) 463.

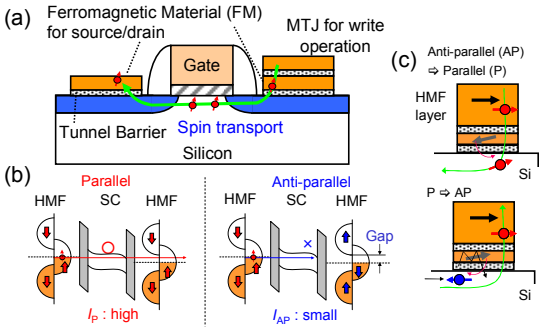

Fig. 1. Novel spin-based MOSFET of "Spin-transfer-Torque-Switching MOSFET (*STS*-MOSFET)". (a) Example of *STS*-MOSFET structure with a magnetic tunnel junction (MTJ) for write operation. (b) Read operation of spin-based MOSFET with highly spin-polarized ferromagnetic electrodes such as half-metallic ferromagnet (HMF) and tunnel barrier. (c) Write operation by spin-transfer torque switching (STS).

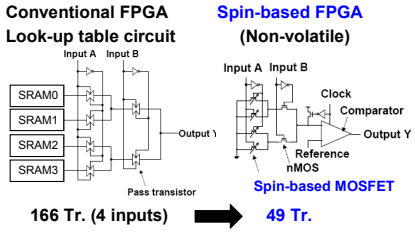

Fig. 2. Spin-based FPGA compared with conventional FPGA. Circuit diagram showing the conventional CMOS look-up-table (LUT) circuit consists of many SRAMs and a multiplexer (left). Proposed LUT utilizing spin-based MOSFET replaces SRAMs and part of multiplexer with spin-based MOSFETs resulting in dramatic reduction of the number of transistors (right).

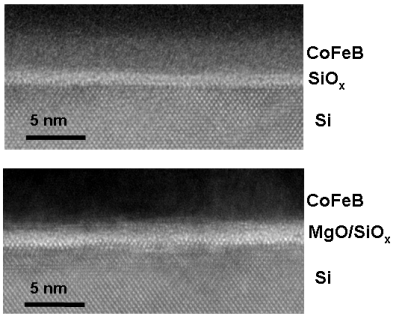

Fig. 3. Cross-sectional high-resolution transmission electron microscope (TEM) image of electrode layer structures consisting of (a) CoFeB/SiOx/Si and (b) CoFeB/MgO (nominal 0.6 nm)/SiOx/Si, along the [110] direction of the Si.

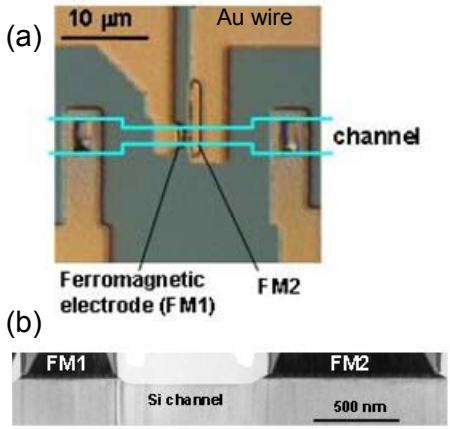

Fig. 6. Device structure for spin injection and detection; (a) optical plane image, (b) cross-sectional TEM image of the electrodes structure on Si.

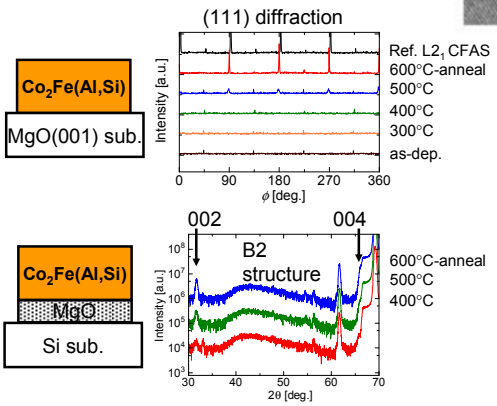

Fig. 8. X-ray diffraction patterns of as-deposited, 300ºC-600ºC annealed full-Heusler alloy $Co_2Fe(Al_{0.5},Si_{0.5})$ (CFAS) films deposited on (a) MgO(001) substrates and (b) MgO-buffered Si(001) substrates; (a) epitaxial $L2_1$ structure. (b) 001-oriented B2 structure.

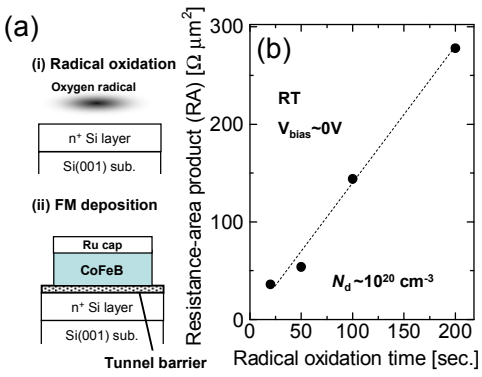

Fig. 4. Radical oxidation for low resistance area product (*RA*) of FM/I/Si junctions; (a) fabrication method and the structure, (b) *RA* vs. radical oxidation time.

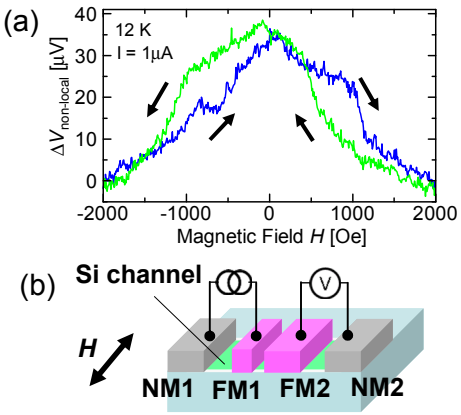

Fig. 7. Spin transport properties through Si channel with the CoFeB/MgO/SiO_x electrodes at 12 K. (a) Non-local signal $\Delta V_{non\text{-}local}$ vs. magnetic field. The junction size was 0.4 × 1 μm and 0.8 × 10 μm. (b) Measurement setup for the non-local signal.

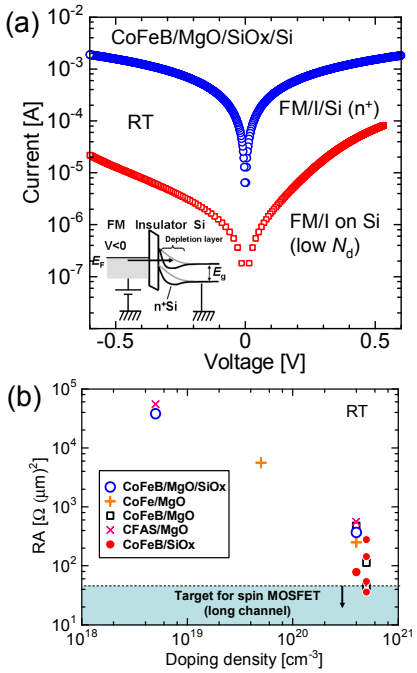

Fig. 5. Electric properties for the fabricated FM/I electrodes on a Si substrate. (a) *I-V* characteristics of CoFeB/MgO/SiOx/Si structures. The bias voltage was applied with respect to Si substrate. (b) Resistance area products (*RA*) vs. doping density in Si with varying FM/I barrier electrodes.

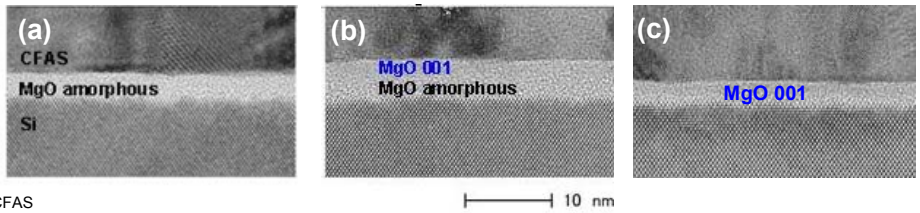

Fig. 9. High-resolution TEM images of CFAS/MgO tunnel barrier on Si(001) substrates. (a) the MgO layer with the thickness of less than 2 nm (nominal) was determined to be amorphous. (b) Thicker MgO (>2 nm) had a 001-oriented crystalline layer and an amorphous layer under that. (c) By using improved condition, crystalline MgO(001) with the thickness of ~1.2 nm was obtained .

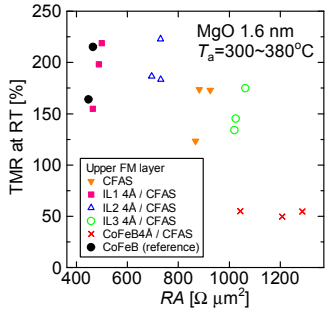

Fig. 10. TMR ratios vs. *RA* values with varying upper electrodes and annealing temperature (*Ta*) for top-CFAS/MgO/bottom CoFeB magnetic tunnel junctions (MTJs) with and w/o interfacial layer (IL) between CFAS and MgO barrier. A high TMR ratio of 223% at RT was obtained for the polycrystalline CFAS/MgO-MTJ with 4Å-thick IL on Si substrate.

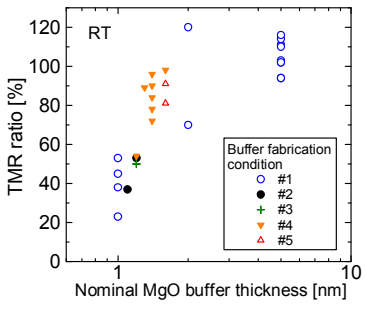

Fig. 11. TMR ratio at RT for CFAS/ MgO (~2nm)/CFAS-MTJ structure on MgO-buffered Si(001) substrates. The TMR ratios depend on the MgO buffer thickness and the fabrication conditions.

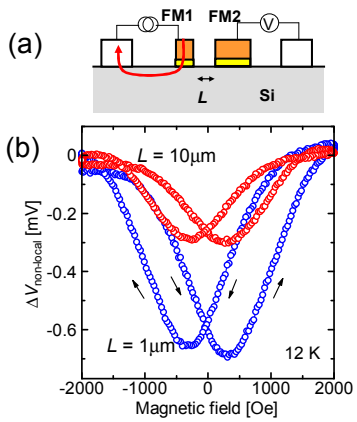

Fig. 12. Non-local measurement in a Si channel with the CFAS/MgO electrodes at 12 K. (a) measurement setup for non-local voltage. (b) non-local curves with the distance L between FM1 and FM2.

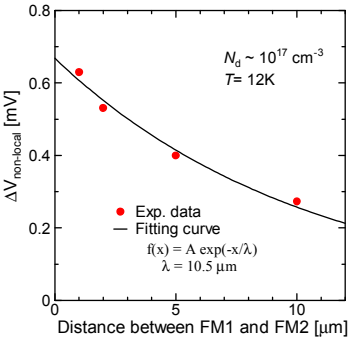

Fig. 13. Dependence of non-local signal $\Delta V_{\text{non-local}}$ on the distance L between FM1 and FM2. By using a fitting curve to the experimental data, a spin diffusion length λ was estimated to be 10.5 μm in the Si-channel of N_d ~5×10^{17} cm^{-3}.

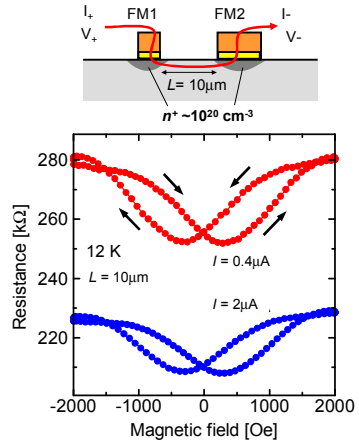

Fig. 14. Spin-dependent transport property, i.e., local-magnetoresistance with the current path of CFAS/MgO/Si channel/MgO/CFAS. The MR ratios of ~10% was observed at 12 K.

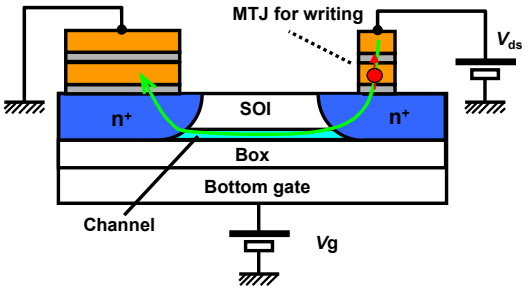

Fig. 15. Schematic view of bottom-gate *STS*-MOSFET fabricated using a silicon-on-insulator (SOI) substrate in this work. Read/write through the SOI channel is operated under the bottom-gate bias V_g.

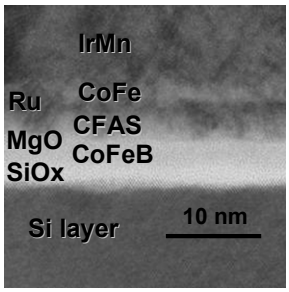

Fig. 16. TEM image for CFAS-MTJ structure on Si. The CoFeB free layer and MgO barrier are thin for spin-transfer torque switching (STS). This image is a magnification of the MTJ in Fig. 17.

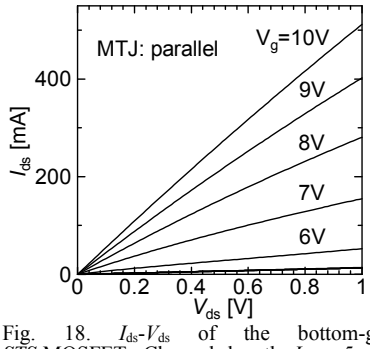

Fig. 18. I_{ds}-V_{ds} of the bottom-gate *STS*-MOSFET. Channel length L = 5 μm, width W = 2 μm. The MTJs are parallel state.

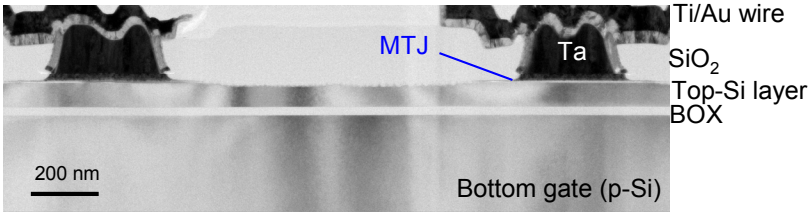

Fig. 17. Cross-sectional TEM image of bottom-gate type *STS*-MOSFET. Two MTJs of CoFeB/MgO 0.85nm/CFAS on a top-Si layer of the SOI substrate are used for the source/drain. The MTJ structure is show in Fig. 16.

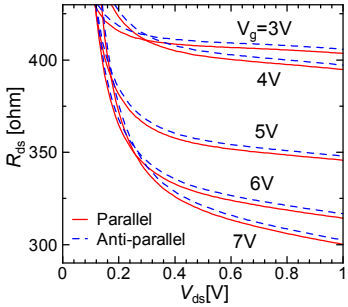

Fig. 19. R_{ds}-V_{ds} of bottom-gate type *STS*-MOSFET. The R_{ds} has two states depending of the magnetization configurations (parallel or anti-parallel) of the MTJ. $R_{ds} = R_{MTJ}+R_c+R_{Tr}$.

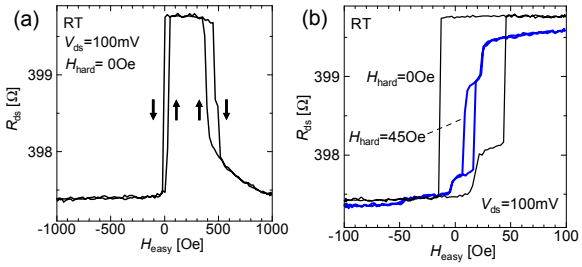

Fig. 20. Magnetoresistance curves of CoFeB/MgO/CFAS MTJ on SOI substrate as a function of magnetic field applied along the easy axis of the MTJ (H_{easy}). The MTJ size is typically 100x300 nm. (a) a typical major loop of the exchange-biased MTJ. (b) minor loops with and w/o the hard axis of the MTJ (H_{hard}).

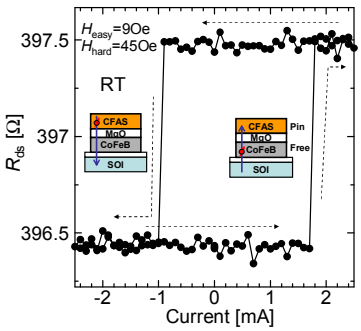

Fig. 21. Spin-transfer torque switching (STS) of the MTJ. The current was applied to the MTJ through SOI channel under V_g = 5V.

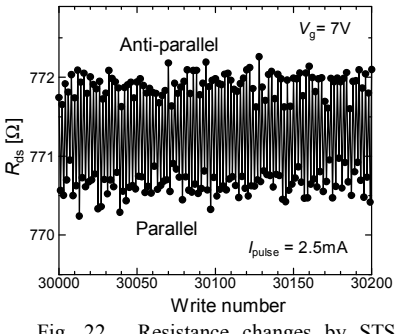

Fig. 22. Resistance changes by STS during 30,000 cycles test in the case that the pulse current of ±2.5 mA and 10 ms duration was applied under V_g = 7 V.